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Design an Efficient Braun Multiplier Using KSA Based CMOS Logics

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Abstract: The addition is the basic process of digital electronics in DSP and VLSI processing applications. In earlier days, many researchers have developed various binary adders and technologies have used to precede the addition process in digital electronic applications. Half and Full Adders are the two fundamental binary adders with limited to the addition up to 3 bits. If the addition required more than 4 bits, then the basic HA and FA adders has not suitable. In that situation, the binary addition process has done with the help of high grade binary carry adders such as RCA, CSA, CSLA, CLA. Due the carry delay problem, the Parallel Prefix Adder (PPA) has selected as the high speed adder to do the binary addition with less delay by researched developers. Generally, the addition is used to implement the binary multiplication process in digital electronics. This paper has proposed the design of Braun Array Multiplier (BAM) using Kogge Stone Parallel Prefix Adder based CMOS logics. Belongs to that, this work has proposed the KSA based Pass Transistor logic, NMOS with Complementary Inverter logic and PMOS with Complementary Inverter logic. All the logics have applied in the Braun Array Multiplier to enhance the performance of multiplication process. The proposed logics have compared with the aspects like area, power and layout size. Microwind tool is able to generate the simulation and analysis results.

Keywords: *Parallel Prefix Adder, Braun Multiplier, Complementary Inverter logic, Kogge Stone Adder, Pass Transistor Logic.*

1. Introduction

A binary multiplier is a digital electronic circuit which is mainly used in DSP, ASIC and VLSI technologies. It is a combinational logic circuit to multiply two binary numbers. The binary multipliers are constructed using binary adders [6]. A several types of arithmetic techniques can be used to design a binary multiplier in digital computer applications. It involved with two values (0's and 1's) and the number which is to be multiplied by the other number is Multiplicand and the number multiplied is Multiplier. A basic 2- bit binary multiplier is acts as the AND gate logic.

In And gate logic, When both the values of inputs are high then the output becomes high and anyone of the input value as low then the output becomes low. Many types of binary multipliers are used in digital electronic applications like Array, Sequential, Booth, Combinational, Logarithm, and Wallace tree multiplier etc. In recent applications of digital signal processing, used the array types of multipliers due to its array calculation of binary adders which leads to high speed process [7]. The multiplication process involved with three steps namely PP (Partial Product) generation, PP reduction and final addition process [10].

The add shift method is the basis for the array multiplier design and its simple in design, regular in shape, minimum complexity. The different Parallel Prefix tree adders, such as Brent Kung, Knowles, Ladner Fischer, Spanning Tree, and Kogge Stone, were established in the earlier [2]. The performance of the PPA design on the basis of delay, area and power in earlier research papers can be used to verify the results [6]. The comparison results show that the PP-KSA created less PDP than other PPA designs [3]. The KSA adder is applied in reverse conversion process of DSP and VLSI applications [8, 9]. Hence, this work is used the KSA based CMOS logics to implement the Braun Multiplier design.

This research paper is structured as follows, in section 2; explained the existing design of Braun Array Multiplier, in section 3; it described the design of PP-KSA with proposed Pass Transistor Logics (PTL), NMOS with Complementary Inverter and PMOS with Complementary Inverter logics, in section 4; it explained the design of Braun Array Multiplier with proposed KSA based CMOS logics, in section 5; It explained the performance comparison results of all

proposed designs. At last, it is concluded based on the comparison results analysis and discussion.

2. Literature Review

In earlier days, the designs of multipliers are done using basic half adders (HA) and full adders (FA). The comprehensive analysis of analysis of PPA is done in existing days [4]. The multiplication process is included with add function and shift operations. The types of multipliers which are used in the multiplication process are discussed in the above section. The type of adders and what are the technologies are used in existing design of multipliers is discussed in the following:

Christian Martyn Jones, et al. (1996) developed the Concurrent error detection using the Braun Array Multiplier's Berger Check Prediction. Berger code is referred to as separable [13]. Using software simulation of an incorrect BAM, all expression correctness has been verified. Deeksha Kiran D K, et al. (2017) implemented Braun Multiplier using full Adder in VLSI technologies. That work is compared for the performance of several FA cells on the aspects of their transistor count (28T, 20T, and 14T) and it used the structure of 4, 8 bit Braun Array Multiplier (BAM) [12]. It employed the cadence tool for 180nm technology for the implementation of layouts.

Seungbum Baek [15] proposed a Memristor CMOS hybrid multiplier used the Braun structure to enable the separation of the multiplier array to initiate multiple multiplication processes simultaneously by changing a control signal on BAM with reconfigurable bit-widths [14]. The proposed structure can work for any high speed and low power array multiplication wanted in VLSI applications. For the implementation process used the FPGA Implementation on Spartan – 3E.

The existing design of Braun Multiplier with various performance results is discussed. The Braun array multiplication is preferred for DSP and VLSI applications due its array calculation of binary addition. The binary multiplication process is done with the help of binary adders [5]. For this work, consider the KSA due to its high speed process. The next section is to design PP-KSA with proposed CMOS logics like Pass Transistor logic, NMOS with Complementary logic and PMOS with Complementary Inverter logics.

3. PP-KSA Design with Proposed Cmos Logics

This section explains the 4 bit PP-KSA with proposed CMOS logics. As the KSA used the less delay, it is preferred in high speed digital electronics applications [1]. Here consider the three proposed logics as: Pass Transistor logic, NMOS with Complementary Inverter logic and PMOS with Complementary Inverter logic. Let's discussed the design of proposed logics design of KSA one by one in the following:

3.1. Pass Transistor Logic (PTL)

By reducing the number of transistors used in a design, this PTL employs several different types of logic gates to transfer logic levels between circuit nodes [11]. The CMOS logic of the pass transistor is designed by the help of both PMOS and NMOS logic circuits. In the 4 bit KSA design, the Carry GP block is applied with Pass transistor logic instead of OR gate logic. For the 4 bit KSA process, A and B input values in the ranges from 0 to 3, Fig. 1 displays the results of the 4 bit KSA design execution using the suggested PTL.

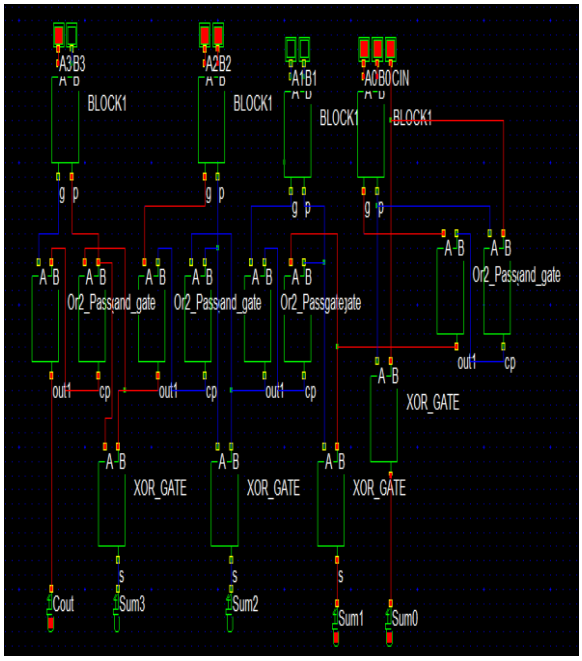

Fig. 1. Execution results of proposed Pass Transistor logic based KSA

In the design itself, given the inputs as A=1101 and B=0101 and Cin =1, the same inputs are given to the waveform verification. In the waveform results, if the input given as high means that indicates the high voltage (1.2V). The KSA with Pass Transistor logic is verified with pulse only not in direct form like normal gate logic. If the given input as low value means, that indicates the zero voltage (0V) in the waveform results. The waveform rests S0=1, S1=1, S2=0, S3=0 and Carry out as 1(high) and the preferred output is obtained with the corresponding inputs. Then the power and area of KSA design is taken with the corresponding inputs.

3.2. NMOS with complementary inverter logic

Any CMOS logic circuits are designed with both p type MOS and n type MOS transistors. In digital circuits, if the inverter gate is used the CMOS (p and n) and all other gates are constructed using NMOS is called the NMOS with Complementary Inverter logic circuits. This proposed logic is applied to design the KSA and explained in this section. The Execution design results of 4 bit NMOS with Complementary Inverter logic based KSA is given in the Fig. 2.

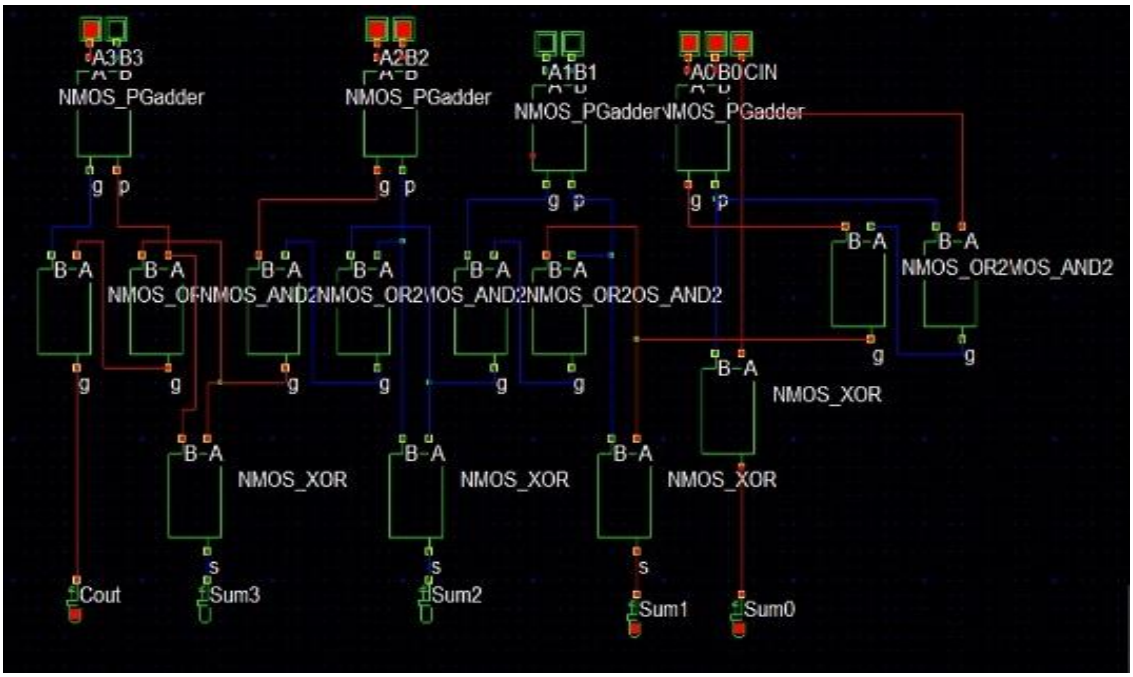

Fig. 2. Execution results of proposed NMOS with Complementary logic based KSA

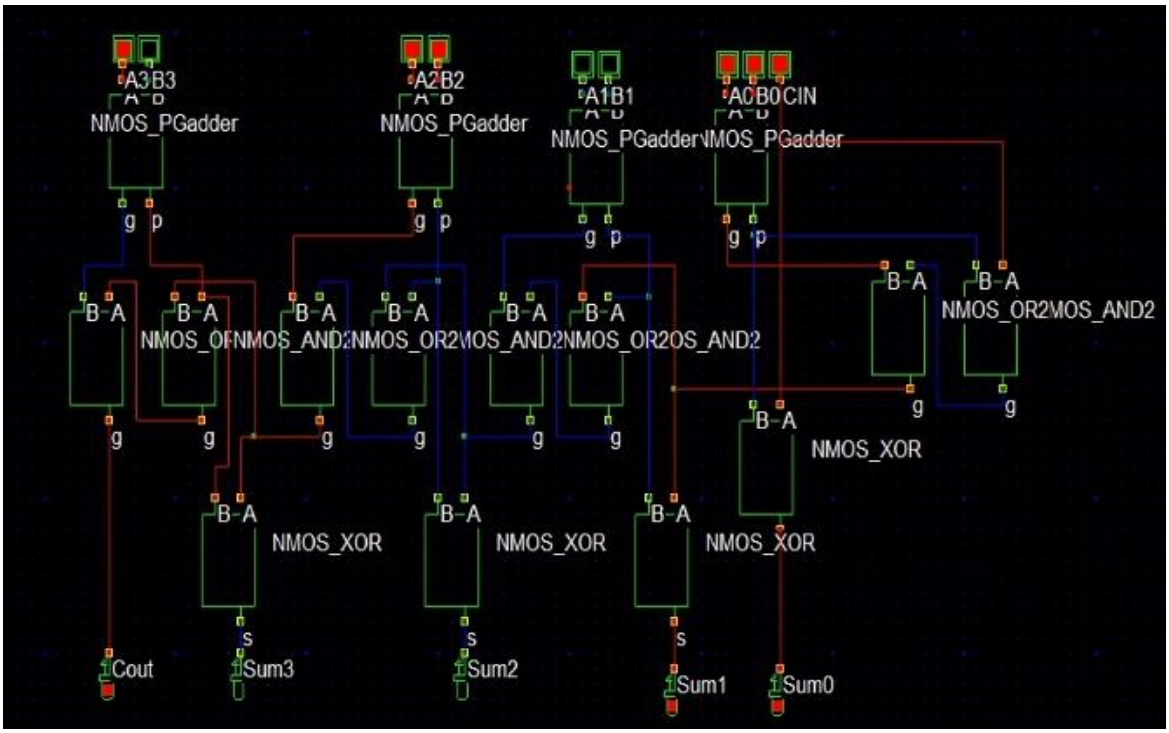

Fig. 3. Execution results of proposed PMOS with Complementary logic based KSA

For this design, given the inputs as A=1101 and B=0101 and Cin =1, the same inputs are given to the waveform verification. In the waveform results, if the input given as high means that indicates the high voltage (1.2V). The KSA with proposed is verified with pulse only not in direct form like normal gate logic. If the given input as low value means, that indicates the zero voltage (0V) in the waveform results. The preferred output is reached in the waveform rests S0=1, S1=1, S2=0, S3=0 and Carry out as 1(high) with the corresponding given inputs. Then the power and area of this KSA design is taken with the corresponding inputs.

3.3. NMOS with Complementary Inverter Logic

In digital circuits, if the inverter gate is used both the p type and n type MOS transistors and all other gates are constructed using PMOS is called the PMOS with Complementary Inverter logic circuits. This proposed logic is applied to design the KSA and explained in this section. The Execution design results of 4 bit PMOS with Complementary Inverter logic based KSA is given in the Fig. 3.

For this proposed design, given the inputs as A=1101 and B=0101 and Cin =1, the same inputs are

given to the waveform verification. In the waveform results, if the input given as high means that indicates the high voltage (1.2V). The KSA with proposed is verified with pulse only not in direct form like normal gate logic. If the given input as low value means, that indicates the zero voltage (0V) in the waveform results. The preferred output is obtained when the corresponding inputs are used to generate the waveform rests S0=1, S1=1, S2=0, S3=0, and Carry out as 1(high). Then the power and area of this proposed NMOS with Complementary logic based KSA design is taken with the corresponding inputs. The comparison analysis of all the proposed logic based KSA designs will be discussed in the fifth section.

4. Braun Multiplier Design with Proposed Cmos Logics Based KSA

In this section, explained the 4 bit Braun Array Multiplier (BAM) with proposed CMOS logics based Kogge Stone Adder. Here consider the three proposed logics as: Pass Transistor logic, NMOS with Complementary Inverter logic and PMOS with Complementary Inverter logic based KSA to design BAM. Let's discussed the design of proposed logics design of KSA one by one in the following:

4.1. PTL based KSA

The Kogge Stone Parallel Prefix Adder is applied in the Braun multipliers instead used of Full Adders for the high speed operation. By lowering the number of transistors that operate as switches to pass logic levels between circuit nodes, this PTL employs a variety types of logic gates in a specific design. The Pass Transistor CMOS logic is designed by the help of both PMOS and NMOS logic circuits.

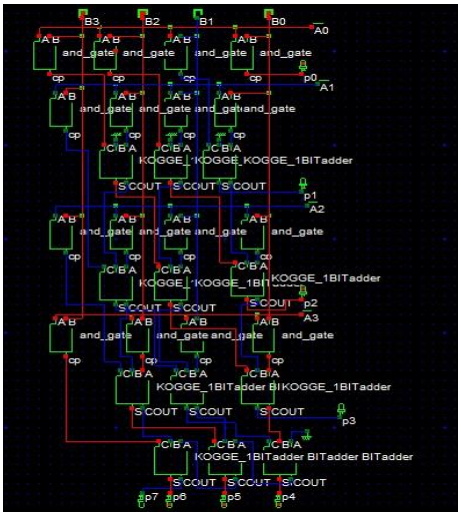

Fig. 4. RGB to YCbCr Conversion

In the design itself, given the inputs as A=1101 and B=1001, the same inputs are given to the waveform verification. In the waveform results, if the input given as high means that indicates the high voltage (1.2V). The KSA with Pass Transistor logic is verified with pulse only not in direct form like normal gate logic. If the given input as low value means, that indicates the zero voltage (0V) in the waveform results. The waveform rests P0=1, P1=0, P2=1, P3=0, P4=1, P5=1, P6=1 and P7=0 with the corresponding supplied inputs results in the preferred output.

BAM with KSA-based NMOS with Complementary Inverter logic

The NMOS with Complementary is mainly used in the design of electronic designs to minimise the usage of PMOS devices. Here this proposed logic is applied to enhance the performance of Braun Multiplier. The AND gate circuit consists of one NAND gate with Inverter (NOT) gate circuit design, here the NAND gate is fully constructed with N-type based devises and the NOT gate involved with both n and p type MOS devices which type of logic is called as NMOS and Complementary Inverter logic design.

The Execution design results of 4 bit Braun Multiplier with KSA based NMOS with Complementary Inverter logic is given in the Fig. 5.

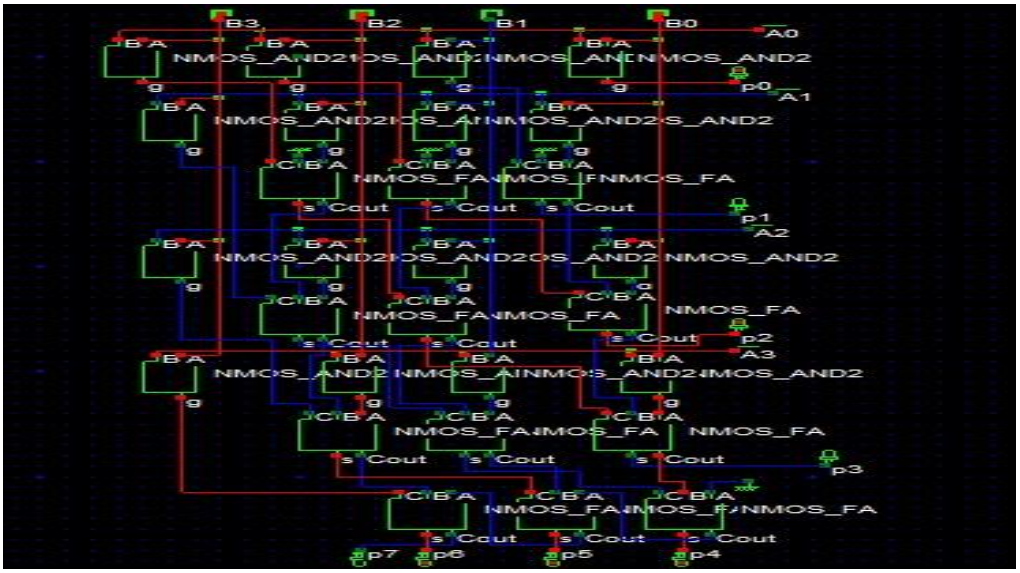

Fig. 5. Execution results of BAM with KSA based NMOS with Complementary logic

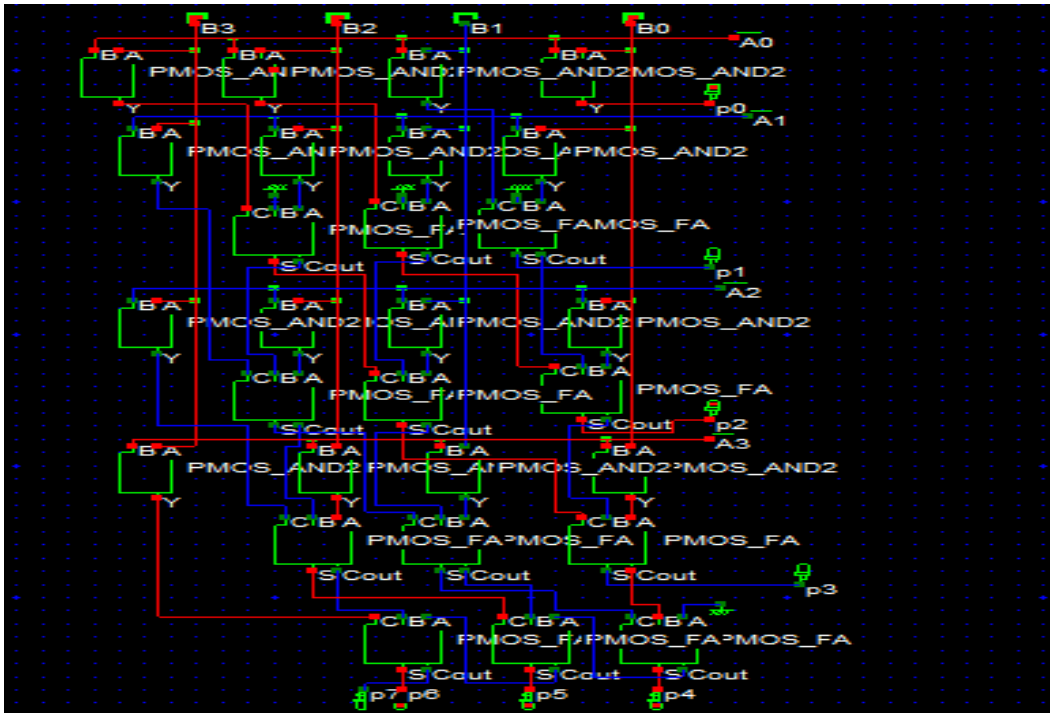

Fig. 6. Execution results of BAM with KSA based PMOS with Complementary logic

In this proposed design, given the inputs as A=1101 and B=1001, the same inputs are given to the waveform verification. In the waveform results, if the input given as high means that indicates the high voltage (1.2V). The KSA based NMOS with Complementary logic is verified with pulse only not in direct form like normal gate logic. If the given input as low value means, that indicates the zero voltage (0V) in the waveform results. The preferred output is reached in the waveform rests P0=1, P1=0, P2=1, P3=0, P4=1, P5=1, P6=1 and P7=0 with the corresponding given inputs.

4.3. BAM with KSA based PMOS with Complementary Inverter logic

The PMOS with Complementary is mainly used in the design of electronic designs to minimise the usage of NMOS devices. Here this proposed logic is applied to enhance the performance of Braun Multiplier. The AND gate circuit consists of one NAND gate with Inverter (NOT) gate circuit design, here the NAND gate is fully constructed with N-type based devises and the NOT gate involved with both n and p type MOS devices which type of logic is called as PMOS and Complementary Inverter logic design. The Execution design results of 4 bit Braun Multiplier with KSA based

PMOS with Complementary Inverter logic is given in the Fig. 6.

The Braun Multiplier is designed with all proposed logics based KSA and the execution results are verified by the design figures and waveform results. Next the performance all BAM designs is compared with area, power and layout size which is given in the next section.

5. Comparison of KSA and BAM Design Performances

The comparison results of PP-KSA design with all proposed CMOS logics and Braun Array Multiplier design with proposed logics based KSA are explained in this section. The performance outcomes have been examined and contrasted in terms of pattern size, power consumption, and area utilisation. All the results of synthesized and simulated are verified using Microwind CMOS tool. Here the threes inputs are applied such as A, B with the ranges (0-3) and Cin. When the block circuit diagram's execution produces the desired results, the LED acts "ON" for high values of -1 and "OFF" for low values of -0. The area consumption report for KSA based proposed PTL is shown in Fig.7. The comparison of the suggested CMOS logics, such as the pass transistor logic, with the KSA design, NMOS with Complementary Inverter logic and PMOS with Complementary Inverter logic is given in the Tab. 1.

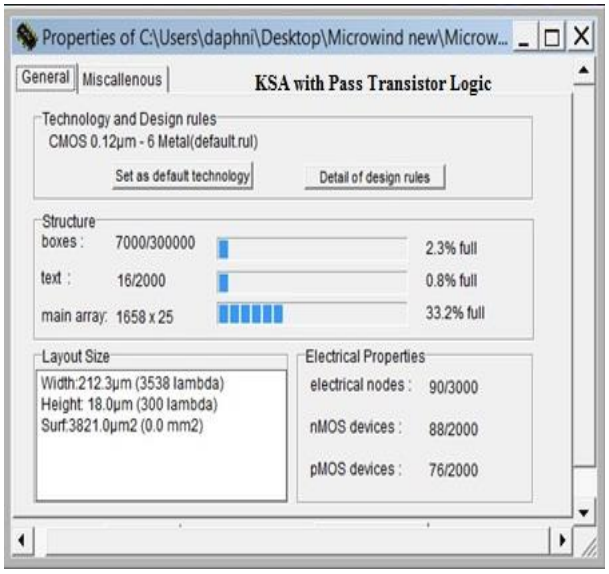

Fig. 7. Area consumption report of KSA with Pass Transistor logic

The area consumption report includes with number of device used and the layout size. The n-MOS devices used as 88 and the p-MOS devices used as 76. The power consumption used by the proposed PTL is 34.027µW. Like this, the area consumption report of all proposed CMOS logics with KSA is taken and the comparison is done with the performances.

Table 1. Comparison results of proposed CMOS logics based KSA design

Designs	Power (µW)	Devices		Layout- size	
		N-MOS	P-MOS	Width	Height
KSA with Pass Transistor Logic	34.027	88	76	212.3µm	18.0µm
KSA with NMOS logic	11.890	68	28	93.2µm	14.6µm
KSA with PMOS logic	39.355	32	72	89.4µm	16.1µm

From the table, when compared to area and the power consumption the NMOS with Complementary Inverter logic based KSA is shown as better than other logics. These three proposed CMOS logic KSA design is applied in BAM and compare the performances and is given in the Tab. 2.

Table 2: Comparison results of proposed CMOS logics based BAM design

Braun Multiplier Designs	Power (mW)	Devices		Layout- size	
		N-MOS	P-MOS	Width	Height
KSA with Pass Transistor logic	0.222	276	276	696.1µm	21.8µm
KSA with NMOS logic	0.191	324	124	408.1µm	22.8µm
KSA with PMOS logic	0.188	148	348	431.2µm	23.3µm

6. Conclusion

An effective 4 bit Braun Multiplier design is done with CMOS logic algorithms. For which, First the Proposed Pass Transistor logic, NMOS with Complementary Inverter logic and PMOS with Complementary Inverter logic is applied in KSA and compared the performances. To enhance the performance Braun Multiplier the KSA based all proposed logics is applied and implemented the BAM design. Based on area and power utility, all of the proposed designs are contrasted. Comparing area consumption to the results of the outcome analysis and the power consumption the NMOS with Complementary Inverter logic based KSA with BAM design is better than other logics. This paper's future action will be to present higher order bit logics in order to achieve extended action with less time.

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