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A Leakage Reduction Charge Pump based Domino Logic for Low Power VLSI Circuits

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Abstract: A new leakage reduction domino logic circuit with a charge pump and a transistor is proposed to improve the performance of the high fan-in circuits. The charge pump and two parallel connected transistors are used to improve the signal strength of the output and reducing the delay. Keeper transistor is used to restore the logic levels of the node. An additional transistor is used to reduce the leakage currents and reducing the power dissipation. The proposed circuit is also applied for domino OR logic function. The proposed technique has a lesser delay and power dissipation compared to the standard domino logic. The proposed technique is more suitable for high speed and low power domino OR logic and can be implemented to the high fan-in gates.

Keywords: *Charge pump, domino logic, leakage reduction, Low power VLSI*

1. Introduction

Low power consumption is essential for deep submicron CMOS based VLSI circuits. The increase in the power consumption of high-performance microprocessors also limits the performance and functionality. Low power operation is also essential for handheld devices for its extended battery life. Logic functions also need to be implemented for higher speed and low power. The performance of domino logic circuits is better compared to static CMOS design, due to its reduced noise margin [1]. Domino circuits are also used in high-speed applications for the implementation of high fan-in circuits. It is necessary to improve the performance of domino logic circuits for driving the high fan-in circuits. Body biasing the transistor also improves the performance of the circuits [2]. A high-speed low power domino logic circuit is proposed. The proposed circuit dynamically changes the threshold voltage of the keeper transistor by biasing the body of the keeper transistor [3]. Another variable threshold voltage keeper circuit is proposed for power reduction and speed enhancement. Here reverse body bias is applied to the keeper for increasing the threshold voltage and reducing the keeper contention current [4]. A novel design combining the low supply voltage keeper technique and low body voltage keeper is proposed. The proposed technique improves the performance of high fan-in domino OR logic [5]. A diode footed domino circuit is designed for high performance, leakage tolerant, and low power. The performance of the proposed circuit is better than the conventional domino logic and is more suitable for scaled CMOS technologies [6]. Low power operation is essential for extended battery life. Devices have to be operated below the subthreshold to reduce power consumption. Operating the devices in the subthreshold region leads to leakage power dissipation. To satisfy these constraints transistors have to be operated at different threshold voltages. A technique for reducing the standby leakage power consumption without affecting the delay and power characteristics at active mode has been proposed [7]. The proposed technique uses sleep switches for reducing leakage and operates at dual threshold voltage [7]. Dual threshold voltage CMOS technology using PMOS sleep transistors reduces the subthreshold and gate oxide leakage in the domino logic circuit [8]. Leakage current characteristics were analyzed in the domino logic circuit. The results show that the conventional CHIH (clock signal and inputs are all high) state is only effective to suppress the leakage current at a high temperature other than high fan-in dominos [9]. The effect of dual threshold voltage technique (DTV) for low power domino logic is analyzed. DTV is more effective in reducing the total leakage and active power consumption for domino gates using different structures [10]. FINFETs are also used in the domino circuits to improve the overall performance of the circuit. A FINFET based process with temperature variation tolerant domino OR gate is designed. The proposed design achieves process and temperature variation tolerance with an increase in layout area [11]. Another low power FINFET based domino OR circuit is proposed. The proposed circuit has a maximum reduction in power consumption compared to the other recently proposed circuits [12]. Another FINFET based domino technique for low power, high speed, and reduced noise have been proposed. The proposed technique uses the current division technique for improving the performance

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parameters [13]. A leakage tolerant domino circuit for low power and higher noise immunity has been proposed. The proposed circuit also utilizes the property of FINFET on the domino circuit for better performance [14]. FINFET based domino logic designs have lesser power consumption compared to the CMOS based conventional domino circuit [15]. Logic functions are implemented using the domino circuits. The Stacking effect reduces the leakage of the evaluation network of domino gates. A new leakage tolerant technique using the stacking effect has been proposed. The performance of the proposed technique is better for higher fan-in gates [16]. A new domino technique based on lector with footed diode inverter is proposed for reducing the gate oxide and subthreshold leakage currents [17]. Noise is another concern in domino logic circuits. A new domino circuit is proposed for higher noise immunity and reduced power [18]. Another domino logic circuit for higher noise immunity is proposed. The stacking of the NMOS transistor reduces the leakage current and power [19]. Noise immunity of domino logic can be improved by controlling the keeper transistor. A separate keeper controlling the network is used to improve noise immunity. This network turns ON or OFF the keeper transistor based on the requirement. The proposed design controls the keeper transistor and reduces delay, power, and improves noise immunity [20]. Controlling the keeper transistor of the domino logic circuit can increase the speed of operation [21, 22]. An additional PMOS keeper transistor is used in the keeper control circuit. This reduces the contention current and leads to high performance [21]. A high speed clock delay dual keeper domino circuit has two keeper devices used to reduce the contention current and increase the operating speed of the device [22]. Domino logic with the combination of current comparison domino logic and conditional high-speed keeper domino logic is proposed. The proposed combination improves the performance of domino logic in terms of delay, power, and noise immunity [23]. CNTFET based domino logic is proposed for the design of low-power domino circuits. The proposed technique has a maximum delay and power reduction compared to the current mirror footed domino logic [24]. A 4:1 multiplexer designed using a dual chirality technique is implemented into the CNTFET technology. The dual chirality technique can change the threshold voltage of the CNTFET based on the requirement. The proposed technique has more improvement in reducing delay and power consumption [25]. The clock gating technique is used to pass and bypass the clock signals for the active mode and standby mode respectively. This reduces the power dissipation in domino logic [26].The major requirement of a domino logic circuit is to reduce the leakage currents and reduce power and delay. In this paper, we have proposed a new domino logic technique using a charge pump and an additional NMOS transistor. The charge pump improves the speed by increasing the voltage at the node. The NMOS transistor is connected such that to suppress the leakage currents and reduce the power dissipation. The proposed domino logic technique increases the speed and reduces the leakage power consumption. In this paper, chapter 2 discusses the working of standard domino logic circuit, chapter 3 discusses the operation of proposed domino logic circuit, chapter 4 consists of results and discussions and chapter 5 concludes the paper.

2. STANDARD DOMINO LOGIC CIRCUIT

Domino logic is developed to speed up the circuits. Domino circuits are widely used in high-speed applications for the implementation of high fan-in circuits [1]. However, domino circuits are vulnerable to noise. The noise sensitivity of domino circuits is due to their low switching threshold voltage, which is equal to the threshold voltage of NMOS devices in the evaluation network. Similar to the CMOS logic, domino logic has full swing voltage. Full swing voltage is essential for higher noise margins. The domino logic is especially used to overcome the problems in the dynamic CMOS gates [1]. Fig 1. Shows the standard domino logic circuit. During the precharge phase, the clock is low, transistor MP1 is ON and transistor MN1 will be OFF. The node N1 is charged to V_{DD}. Node N1 is connected to inverter IN1. The Output of IN1 V_{out} becomes low. V_{out} is directly connected to the gate of the keeper transistor MP2. Since V_{out} is low, transistor MP2 will also be ON and restore the node N1 to V_{DD}. During the evaluation phase the transistor MP1 is OFF and MN1 is ON and discharges the node N1 to low state. A low state to N1 also forces V_{out} to a high state and turning off the keeper transistor MP2.

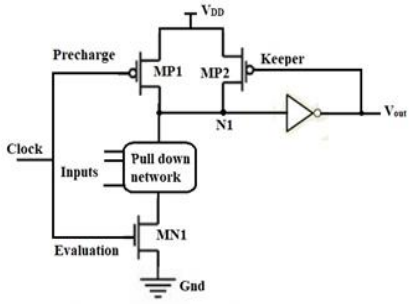


Fig 1. Standard domino logic circuit

The major issue during the evaluation phase is the leakage currents that flow through the pulldown network despite the inputs in the pulldown network. These leakage currents induce power dissipation.

3. PROPOSED DOMINO LOGIC CIRCUIT

The circuit is divided into two sections, input section has precharge transistor MP1, inverter IN2, footer transistor MN1 and pulldown circuit of the logic to be implemented whereas the output section consists of a keeper transistor MP2, static inverter IN1, transistor MN2 for leakage current reduction, capacitor C_1 act as a charge pump and transistor MP3 and MP4 connected in parallel. Fig 2. Shows the proposed domino logic circuit. During the precharge phase, the clock is low transistor MP1 is ON and MN1 is OFF. Transistor MP1 pulls the node N1 to V_{DD}. The node N1 connected to IN1 forces the output V_{out} to low. The output of V_{out} connected to the gate of MP2 turns on MP2 and node voltage N1 stays at V_{DD}. At the same time the output of IN2 is high which starts charging the capacitor C_1. Capacitor C_1 act as a charge pump. The node voltage N1 at high state turns off MP3 and MP4 and turns on the keeper transistor MN2. This passes a low input to the node N2. There is no chance of leakage currents from MP3 or MP4. The signal flow is also faster. The transistor MN2 is ON and suppresses the leakage currents by passing a logic 0 to the node N2. During the evaluation phase clock is high MP1 is OFF and MN1 is ON, pulling the node voltage N1 to low

based on the inputs of the pulldown network. A low at node N1 turns on the transistor MP3 and MP4 and turns off MN2. At the same time IN2 is forced to low state. A high to low transition discharges the capacitor C_1 towards node N2 also increasing the node voltage. The transistor MP3 and MP4 force the output voltage Vout to high state with its increased node voltage and reducing the delay. Now MP2 is OFF and maintains a low signal at node N1. This also forces the output Vout to logic 1. At the evaluation phase the transistor MN2 is isolated and MP2 is turned OFF. The output is forced to a high state by a parallel connected transistor that reduces the delay and dynamic power. The transistor MN2 passing a low signal to node N2 during the precharge phase and isolating the transistor MP3 and MP4 from the node voltage at N2. This reduces the leakage currents.

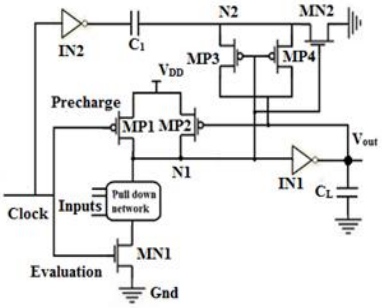
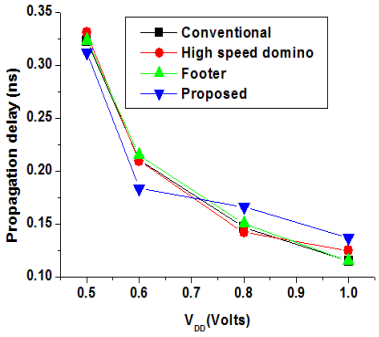


Fig 2. Proposed domino logic circuit

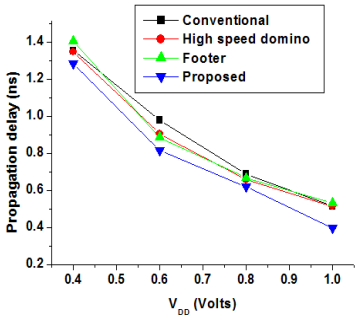
During the precharge phase, transistor MN2 is ON and blocks the signal from MP3 and MP4 and reducing the leakage. During the evaluation phase MN2 and MP2 are OFF. The output depends upon the transistor MP3 and MP4 with a boosted node voltage at N2. This increases the speed of the signal to the output and also completely able to turn OFF the keeper transistor MP2. The transistor MN2 is used to suppress the leakage current and reduce power. The proposed circuit controls the keeper transistor MP2 from turning ON during evaluation and also boosting the signal using a charge pump and reduces the delay and leakage power.

4. Results and Discussions

This section gives the results of the proposed domino logic circuit. To evaluate the effectiveness of the proposed technique, delay, power dissipation, power delay product of the proposed technique is compared with the standard domino logic (conventional), high-speed domino logic [13], and Lector with footed diode inverter [17]. The simulations are done at the 22nm technology node using spice software. The simulations are also extended for OR gate logic and their performance is also analyzed.



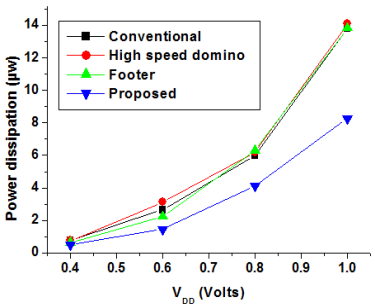
(a)



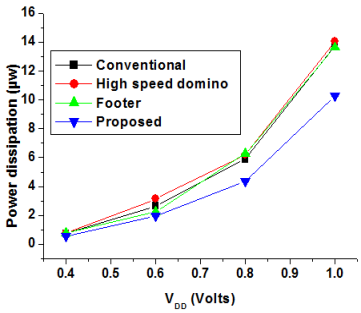
(b)

Fig. 3. Comparison of voltage and propagation delay for various load capacitances (a) C_L=1fF, (b) C_L=4fF.

Fig. 3. shows the comparison of voltage and propagation delay for various load capacitances. Scaling the voltage for reducing power increases the propagation delay. The propagation delay of the proposed domino logic is lesser for lower voltages compared to the standard domino logic and other domino logic styles. Fig. 3(a) to 3(b) shows the comparison of voltage and propagation delay for the load capacitance from C_L=1fF and C_L=4fF. From the figure it is inferred that the propagation delay of the proposed domino logic is also lesser for lower voltage and higher load capacitance. This proposed domino logic is suitable for low power and higher load. This is mainly due to the transistor N2 used to reduce the leakage current and the charge pump is used to boost the signal strength of the proposed circuit to reduce the delay.



(a)

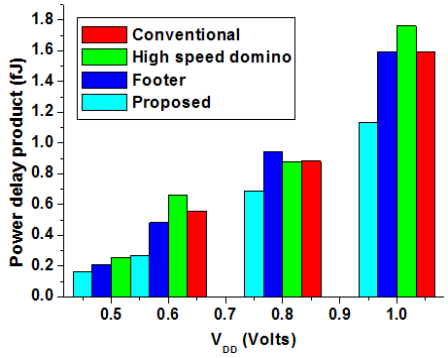


(b)

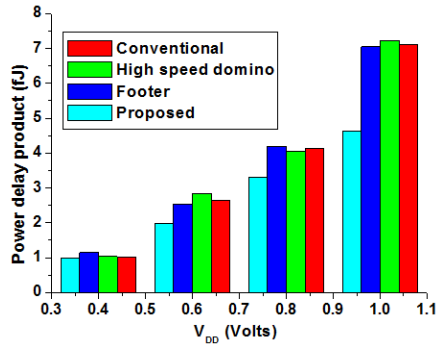
Fig. 4. Comparison of voltage and power dissipation for various load capacitances (a) C_L=1fF, (b) C_L=4fF.

Fig. 4. shows the comparison of voltage and power dissipation for various load capacitances. The proposed domino logic has lesser power dissipation for any voltages and higher load capacitances compared to the standard domino logic circuit and other domino logic circuits. This is due to the transistor N2 which passing a low

signal whenever it is ON and thereby reducing the leakage currents and reducing the power dissipation. Fig. 5 shows the power delay product of the proposed domino logic with the standard domino logic, high-speed domino logic [13], and Lector with footed diode inverter [17]. The power delay product of the proposed domino logic is better than the other domino logics for lesser voltages and higher loading conditions. The proposed domino logic is more suitable for subthreshold operation. The proposed logic is also extended for the two input OR gate by varying the load capacitance for a supply voltage of V_{DD}=0.5V.



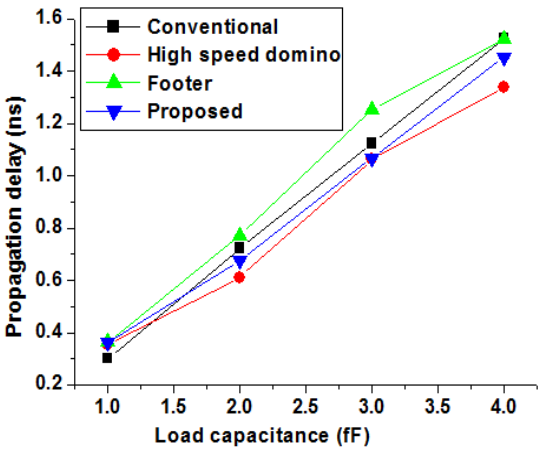
(a)



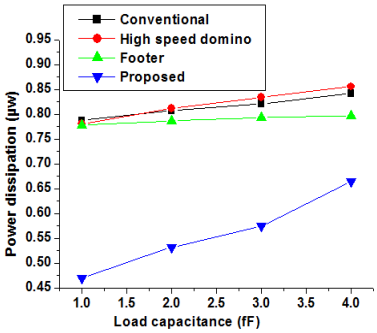
(b)

Fig. 5. Comparison of voltage and power delay product for various load capacitances (a) C_L=1fF, (b) C_L=4fF.

The performance of the proposed logic is verified by increasing the fan-in conditions. The load capacitance is increased for higher fan-in conditions. The simulation is done by varying load capacitance, the delay and power dissipation performances are analyzed. While increasing the load capacitance for OR domino logic the propagation delay increases linearly.



(a)



(b)

Fig. 6. Comparison of Load capacitance with (a) propagation delay and (b) power dissipation for two input OR domino logic.

Fig. 6(a) show that the propagation delay of the proposed domino logic is lesser than the standard domino logic and lector with diode footed inverter [17] and propagation delay is higher than high speed domino logic [13]. Fig. 6(b) shows that the proposed domino logic has lesser power dissipation compared to the standard domino logic and other domino logic. The reduction in power dissipation is more compared to other domino logic. This is due to the reduction of leakage current in the proposed domino logic. Table. 1 shows the comparison of power delay product for OR domino logic functions by varying the load capacitance. The proposed domino logic has a lower power delay product compared to the standard domino logic and other domino logic function for higher load capacitance.

Table 1. Comparison of power delay product for OR domino logic.

Load capacitance (fF)	Standard domino logic	High speed domino logic [13]	Lector with footed diode [17]	Proposed
1	0.236	0.273	0.283	0.170
2	0.583	0.515	0.607	0.360
3	0.922	0.902	0.994	0.613
4	1.284	1.161	1.213	0.966

These results show that the proposed domino logic is more suitable for implementing the logic functions at the subthreshold region and higher fan-out conditions.

5. Conclusion

A new leakage reduction circuit technique is proposed for a higher fan-in domino logic gate. The delay is reduced by using the charge pump and increasing the input voltage of the PMOS transistor to increase the signal strength. Power dissipation is reduced by reducing the leakage currents using an additional transistor. The proposed circuit controls the input of the keeper transistor. The proposed technique is also applied for two input domino OR gates. The power delay product of the proposed domino OR gate is lesser than the standard domino OR logic, high speed domino logic, and lector with footed diode logic. The proposed circuit is more suitable for wide fan-in OR gates and can be used for high speed and low power applications.

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