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OOK Modulation Using intelligent OMIC Less Power Aware Clocked Threshold Inverter Quantized Flash ADC

P. Brundavani[1], D. Vishnu Vardhan[2]

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Abstract: Because it connects the analog physical world and the digital logical world, an analog-to-digital converter, also known as an ADC, is a fundamental component of system-on-chip (SoC) products. System-on-a-chip (SoC) uses of CMOS flash ADCs benefit from threshold inverter quantization (TIQ). TIQ is a method that use a voltage comparator built from two cascaded CMOS inverters. The recent developments in SoC design need the development of this TIQ technique to accommodate the increased integration of ADCs with other electrical circuits on the chip and the increased emphasis on low-power and low-voltage uses. This idea addresses the need for an analog-to-digital (ADC) converter that is both efficient and upgraded for the coherent detection of On-Off Keying (OOK) methods. A modulation strategy known as on-off keying, or OOK, involves turning on and off a sinusoidal carrier signal with a unipolar binary signal. This is done in order to create a modulated signal. OOK is analogous to the amplitude-shift keying (ASK) technique that uses two levels. OOK modulator If there is a zero to transmit, the RF carrier should simply be turned off, and if there is a one, the carrier should be sent at full power. The ADC design technique is cutting edge; it does away with the resistor ladder entirely, which brings about a significant reduction in the power demand of an analog to digital converter.

Keywords*: Witched inverter scheme (SIS), sleep transistor, OOK, modulator, demodulator, CMO, millimeter-wave, quantization noise.*

1. Introduction

The flash-type A/D converter architecture is the most desirable alternative for high-speed A/D converter design; yet, it is inefficient for resolutions more than 8 bits from the standpoints of power consumption and size[1]. With a low enough resolution, the number of comparators can be kept manageable, and their offsets don't have to be particularly precise. Comparator structures are therefore the most important components of full-flash type topologies.

The following is a list of some of the issues that are associated with the standard comparator structures that are utilized in A/D design:

- A huge transistor area, which results in a higher degree of accuracy
- DC bias requirement
- mistakes caused by charge injection
- metastability errors
- a significant amount of power used
- Resistor or capacitor array required.

The Threshold Inverter Quantizer, or TIQ, gets rid of the resistor array implementation that is used in typical comparator array flash designs. Full-flash CMOS inverters' transistor counts are the basis of TIQ[2]. As a result, there is no requirement for static power consumption in order to quantize the analog input signal, which makes the idea particularly appealing for applications that are powered by batteries. Nevertheless, the TIQ technique has five major drawbacks, which are as follows:

- This construction only has one entrance point.
- It requires 2^n-1 distinct area sized quantizer designs.
- A dedicated 5V reference power supply voltage is needed for the analog component alone because of the low power supply rejection ratio.
- As a result of alterations in the process parameters, there are minute shifts in the linearity measures (DNL and INL), as well as the maximum analog signal range. Front end signal conditioning circuits are equipped to address these issues with relative ease.
- It requires S/H to be present at the analog input in order to improve performance while also lowering the amount of power that is consumed during the metastable period.

On-Off Keying (OOK) is a modulation technique that is gaining popularity because to its ability to reduce power consumption and increase operational lifespan in energy-constrained wireless applications [3]. Noncoherent OOK strikes a good balance between low power consumption and a straightforward receiver design. Quantization noise (QN) in the analog-to-digital converter (ADC) slows

1 Department of ECE, Jawaharlal Nehru Technological University Anantapuramu – 515 002, Andhra Pradesh (India)
2Department of ECE, Jawaharlal Nehru Technological University Anantapuramu – 515 002, Andhra Pradesh (India)
Corresponding author: P. Brundavani (e-mail: brundavenky777@gmail.com)

down analysis, though. Although OOK is commonly used in low-power systems, the research is unclear on the appropriate word length of the ADC and the effect of the QN on system performance as a whole [4]. It is common knowledge, however, that the ADC's power consumption scales linearly with sampling frequency and exponentially with word length [5]. Therefore, the study will center on the ADC's word length as a means to guarantee a low-power solution. When designing a system with a restricted power budget, it is crucial to avoid over-designing the ADC. Data converters are needed to interface the signals of the physical world for different applications and then process the received information in the digital domain. A separate circuit for data conversion is no longer an option, and instead an Analog to Digital Converter (ADC) must be constructed on the same chip. Since a few years, there has been intensive study into improving data converters for both speed and efficiency [8]. The need for low power dissipation in many contemporary battery-operated applications is growing as technological advancements continue to be scaled up. Due to its ease of use, a self-heterodyne structure based on OOK modulation has the potential to alleviate power concerns in portable electronics . There is no PLL that requires a significant amount of DC power to operate. A receiver also lacks a local signal source, such as a VCO. These enhancements lessen the 60GHz transceiver's DC power dissipation.

Here is how the rest of the paper is structured. Section 2 defines the literature review of the existing methods. Proposed OOK Modulator using ADC model is discussed in section 3. Section 4 analyse the results and analysis. Finally, section 5 defines the conclusion of the proposed work.

2. Literature Survey

It is common knowledge, however, that the ADC's power consumption scales linearly with sampling frequency and exponentially with word length. Therefore, the study will center on the ADC's word length as a means to guarantee a low-power solution. It is vital to not over-design the ADC when creating a system with a limited power budget. An analytical equation for the error probability in OFDM systems is provided in [6], assuming the QN follows a Gaussian distribution. This presumption holds true for systems with a high number of carriers, but it has no bearing for systems with only one carrier. Under the assumption that the ADC QN is normally distributed, the bit error rate formulae for M-ary pulse amplitude modulation (MPAM) and quadrature phase-shift keying (QPSK) are given in [7]. However, this approach only applies to non-coherent OOK detection and not to coherent MPAM or QPSK detection [8].

There has been a lot of research into the efficacy of non-coherent OOK without QN, and these studies may be found in places like [9] and their citations. The noise shaping property of a delta-sigma modulator, along with the high resolution and distributed pipelined quantization of the suggested modulator, results in an effective tool. Therefore, less integrator gain, swing, and slew is required [10]. The latency introduced by the pipelined quantization is exploited by the modulator to improve the shape of noise. Reduced power consumption, improved stability, and sharper images are the results of these benefits. Emerging applications like Wireless Sensor Network (WSN), neural recording system (NRS), RFID, etc. do not necessitate high performance, but others like CMOS image sensors do. However, they have extremely high standards for energy efficiency. An area of ADC design space, such as ultra-low power, moderate resolution, and speed, is the target of this study. These ADCs are essential in large-scale WSN because they serve as the interface between the perceived environment and the network as a whole, making their performance and adaptability crucial. Despite having a nominal voltage of 1.5 V, the actual operating voltage of an AA Alkaline battery is between 1.65 V and 0.8 V. Its energy density is roughly 1500 joules per centimetres cubed, and it occupies a volume of merely 8.5 cm3. While alkaline batteries provide a low-cost, high-capacity energy source, their broad voltage tolerance range and bulky form factor are two main downsides. Battery self-discharge also makes lifespan longer than 5 years impossible. Lithium batteries, on the other hand, are a source of power that is highly portable. It has a density of 2400 J/cm3 and occupies just 1 cm3[11].

In addition, the voltage they deliver remains very stable even when the battery is depleted. Low nominal discharge currents are a common issue with lithium batteries. Batteries that use nickel metal hydride are the third most common kind. They may be charged quickly and conveniently. One major drawback of rechargeable batteries is the dramatic drop in energy density that occurs over time. Ni-MH batteries, which come in the AA format, cost almost five times as much as alkaline batteries yet only provide 1.2V of energy. It may not be viable to run the system solely on rechargeable batteries due to the high voltage requirements of several of its components. We introduce a 1-GS/s, 8-bit, two-stage SAR ADC [12] that uses partial interleaving. Background calibrations address both the gain error and the comparator offset. The 2.1 mW of power required from a 2.2 V supply allows the ADC, which is manufactured using a 28 nm FDSOI technology, to achieve an SNDR of 46.65 dB at Nyquist at a sampling rate of 1 GS/s.

This article by Thai H-H (2023) offers a low-area 8-bit flash ADC that uses less power and takes up little space. An analog multiplexer (MUX), a comparator, an encoder, and an SPI (Serial Peripheral Interface) block are the four primary components that make up the flash ADC. A selection can be made between all eight analog inputs thanks to the MUX. In addition to a control circuit and a proposed architecture for a Double-Tail (DT) comparator, the comparator block features a TIQ comparator, which stands for threshold inverter quantization. By utilizing the DT comparator, one may cut the total number of comparators in half, which in turn helps to cut down on the overall size of the design area. A straightforward link between the ADC and the microcontrollers can be made available by the SPI block. The CMOS technology used for the design and simulation of this mixed-signal circuitry has a resolution of 180 nm [13]. There are only 128 comparators utilized by the 8-bit flash ADC. The input clock frequency that is being used is 80 MHz, and the voltage can be anywhere from 0.6 V to 1.8 V. The temperature readings are transmitted to the encoder through a 127-bit code generated by the comparator block. The encoder then exports the seven bits of the binary code that are considered to be the least significant. The value of the most significant bit, often known as the MSB, is determined by a single DT comparator. On average, 2.81 milliwatts of electricity are drawn from the supply by the design. 0.088 mm2 is the entire area of the arrangement as a whole. Approximately 877 fJ/step constitutes the figure of merit (FOM). Following completion of the research, a chip will be created and have the design embedded into it.

In applications of system-on-chip (SoC) that rely on CMOS flash analog-to-digital converters (ADC), threshold inverter quantization (TIQ) is used. The TIQ method is a voltage comparator that employs the utilization of two CMOS inverters connected in cascade. However, in order to accommodate the most recent trends in SoC, this TIQ approach will need to be developed. Because of the rise in importance of low-power and low-voltage applications, ADCs now need to be integrated with other electrical circuits on the chip. Changes in the process, temperature, and power supply voltage were mitigated by the TIQ comparator. This allowed us to enhance the TIQ flash ADC's speed and resolution. Power loss was successfully mitigated by the TIQ flash ADC. Chanakya Dharani (2019) achieves significant reductions in power consumption through careful management of the power dissipation in the comparator [14]. In addition, in comparison to the TIQ comparator, the new comparator offers significant improvements in terms of both its power dissipation and noise rejection capabilities. According to the findings, the TIQ flash ADC based on Modied mux is capable of high-speed transformation, despite its diminutive size, low power dissipation, and low-voltage operation. These characteristics set it apart from other flash ADCs.

No digital signals can be found; only analog ones. To translate between the analog physical world and the digital logical world, a system-on-a-chip (SOC) must have an A/D converter [15]. The reason for this is that it is the bridge between our world and theirs. As the channel length of the MOSFET gets smaller and smaller, it becomes increasingly important to meet the demand for low power and low voltage. An analog-to-digital converter's power and speed can be greatly improved by using a comparator, a crucial component. This study proposes the use of Threshold Inverter Quantization (TIQ) comparators in a low-power, 4-bit flash analog-to-digital converter (ADC) for system-on-a-chip designs. Unlike other quantization techniques, threshold inverter quantization doesn't require a resistor or capacitor ladder circuit because it uses two cascaded CMOS inverters as a comparator [16-22]. Quantization allows the threshold inverter to be built more quickly, with less energy, and in less space. In contrast to digital inverters, which are quick and easy to design, TIQ eliminates the need for high-gain differential-input voltage comparators. TIQ-based flash ADC obviates the need for a resister ladder circuit, which is often used to generate reference voltages. The threshold voltage serves as the reference voltage in the TIQ-based flash ADC, which compares the input voltage to the threshold voltage. This comparison produces the thermometer code. The reference voltage is created internally by the circuit. A transmission gate that is based on a 2*1 multiplexer has been utilized in the design of a very effective thermometer to binary converter. Reduced power consumption in accordance to threshold voltage, with the need that high-speed transistor size be maintained at a minimum. Where n is the number of bits or resolution, the TIQ-based flash ADC requires comparators with a ratio of 2n-1. Keeping the threshold voltage stable and keeping WP/Wn close to 1 can help reduce the design's power consumption. This will help cut down on both power usage and peracetic capacitance.

3. Proposed OOK Modulator using ADC Method

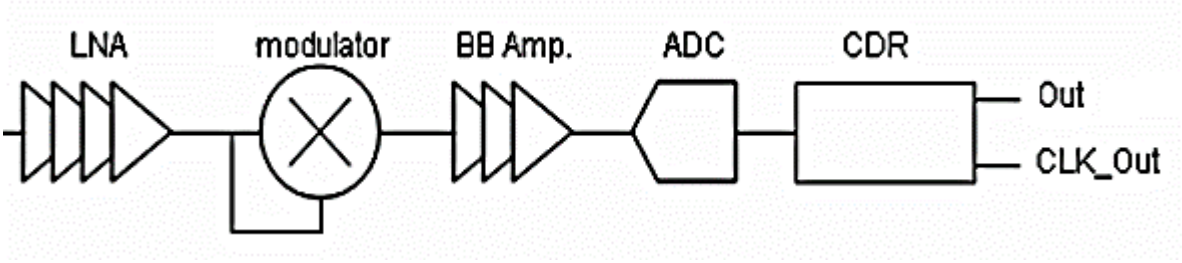

Fig 1: Proposed OOK Modulator using ADC

This receiver stands out from the crowd because of its ability to demodulate signals using coherent direct conversion. Due to the elimination of the need for a local oscillator (LO) and a synchronization technique, often a phase-locked loop (PLL), DC power and complexity are saved. The cost in the demodulator's conversion efficiency will be considerable. A high-gain 60 GHz LNA will serve as the first link in the down-conversion chain. Having a lossy device in the front end, such as the demodulator, increases the noise floor, hence a large gain from the LNA is necessary to compensate. To demodulate the incoming OOK modulated millimetre wave signal back into an analog baseband signal, a 60 GHz direct-conversion demodulator will be used. The signal swing must then be amplified by a baseband amplifier before it can be collected by the ADC and transformed to digital data. To fix the DC offset problem brought on by direct-conversion, huge DC blocking capacitors will be installed in the baseband. In the end, a clock and data recovery circuit will handle the digital information in case it needs to be timed before being transferred to a back-end CPU.

3.1. LNA

Noise was reduced by operating the devices at a current density of 0.2 mA/m, which is optimal in terms of noise performance and maximum frequency of oscillation (fMAX) [10]. This size of device was chosen so that the optimum noise matching and power matching impedances were close to each other. The size of the transistors used is also determined by the need to minimize DC power usage. Low frequency oscillation is dampened by RC networks at the sub ends.

The design of the LNA requires a power match at the input, but that alone is not enough. To ensure that the output signal-to-noise ratio (SNR) does not suffer an unacceptable amount of degradation attributable to the circuit itself, it is essential for a low-noise amplifier (LNA) to meet the noise performance criteria. Therefore, in order to clearly clarify the principle of operation and determine the restrictions on noise performance, a rigorous noise analysis of the capacitive feedback matching approach is constructed. We did this to determine where the ceiling was for noise performance. The research will go more smoothly if you take a brief peek at the commonly-used CMOS noise sources.

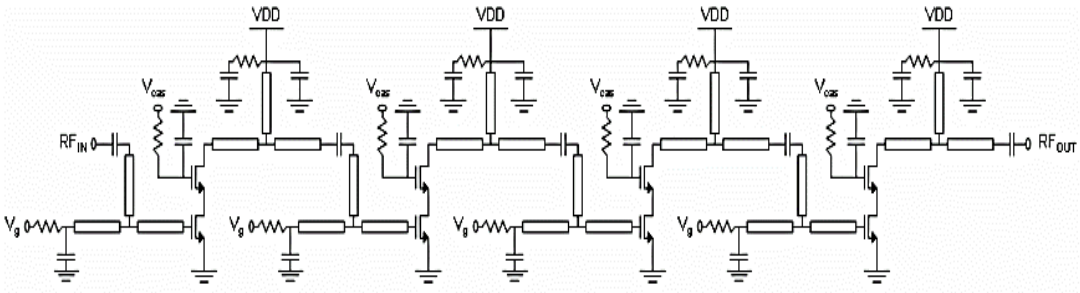

Fig 2. LNA schematic

3.2.OOK MODULATOR

An OOK modulator has strong on/off isolation, high gain in the on state, low DC power consumption, and a high data rate.

"On-off keying," or "OOK," is the simplest kind of "amplitude-shift keying," or "ASK," a method of modulating digital data by describing it as the presence or absence of a carrier wave. The presence of a carrier for a specific time interval represents a binary one, while the absence of a carrier for that same interval represents a binary zero. This concept is expressed in its most basic form. In some more complex schemes, the lengths of these intervals are varied to provide extra information. The unipolar encoding line code is comparable to this format.

Although on-off keying (also known as CW (continuous wave) operation) is the way most commonly used to transmit Morse code over radio frequencies, any digital encoding scheme may in theory be used. OOK has been used in the ISM bands for a number of applications, such as the transmission of data between computers.

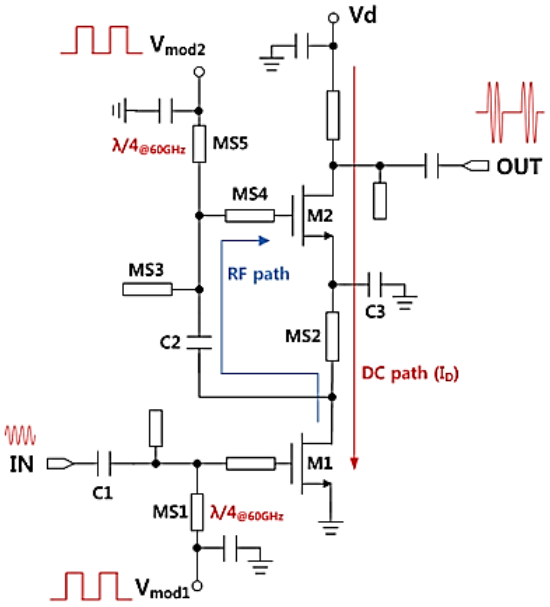

Fig 3: OOK Digital Modulator schematic

Below is a picture of the suggested modulator, which is based on a switching amplifier. Using a current re-use method between two cascading CS (M1 and M2) structures lowers the DC current usage. Dual modulation is used to send the OOK information into the gate biases of both M1 and M2 at the same time. The OOK modulator achieves a high on/off isolation even with very little data by disabling the common source stage in a cascode used as the current source of an amplifier when the data is 0. By replacing the resistor in the gate bias with a quarter-wavelength transmission line (MS1 and MS5), we may decrease the time constant and prevent the 60GHz signal from leaking into the bias. As a result, the modulator is better able to handle the Gbps data rate, as the distortion in the OOK input data is reduced.

3.3. OMIC LESS SWITCHED INVERTER ADC

A precision voltage regulator, not depicted on the schematic, is a portion of the converter circuit that supplies a stable reference voltage, Vref. Each comparator's output will become saturated and high when the analog input voltage rises over the reference value. When there are many active inputs, the highest-order active input is used to generate a binary output via the priority encoder.

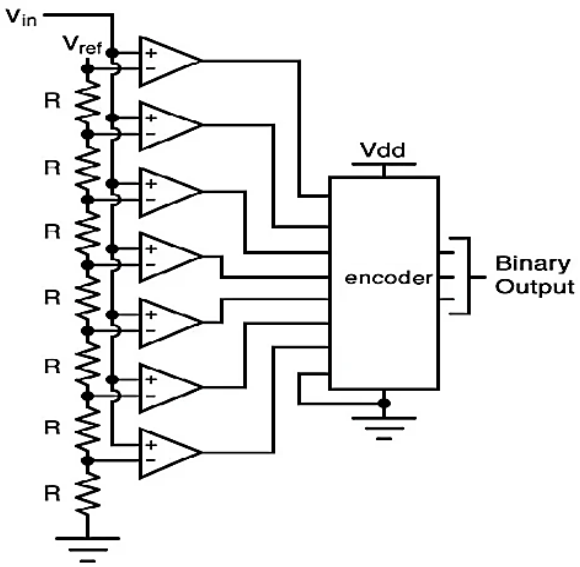

Fig 4: FLASH ADC

In the Flash analog to digital converter, the analog input voltage is compared with all of the comparators' reference values. Following the comparison, we found that the reference voltages of the first three comparators, namely 1V, 2V, and 3V, are lower when compared to the input voltage of 3.3 V. This explains why the output of the first three comparators is high while that of the rest is low.

These outputs will be fed into the priority encoder through its inputs. Since we can count seven of these reference voltages, the eighth input line is tied to logic 1, where it receives the lowest priority. This indicates that the encoder uses a descending order priority format. This is helpful in the scenario in which the output voltages of all of the comparators are zero. As a result, the encoder will give more weight to the outputs with a higher priority, which will result in an output that is entirely zero.

Because all three of the encoder's input lines are active at the same time, the third input will be given precedence, and the encoder will generate a binary code that corresponds to it as a result.

- **Sample & Hold Circuit:** An analog-to-digital converter in Flash goes through this procedure in order to transform a continuous analog input into a binary output. The result of this procedure is a binary output. If you want this ADC to be accurate, the voltage at its input can't have any fluctuations; otherwise, it will have an effect on the output and cause errors. In order to circumvent this problem, a sample and hold circuit is utilized in conjunction with the Flash ADC. The respective circuit takes a sample from the input circuit and stores it until the conversion is finished and the subsequent signal arrives.
- **Half Flash ADC:** It is the version of complete flash ADC that has been optimized. The full-flash analog-to-digital converter (ADC) configuration has an advantage over this setup in that it consumes less power and requires less die space to achieve the same level of resolution.

3.4. SIS COMPARATOR WITH SLEEP TRANSISTOR

The SIS comparator's comparison circuit has high-threshold PMOS and NMOS added to the supply rails.

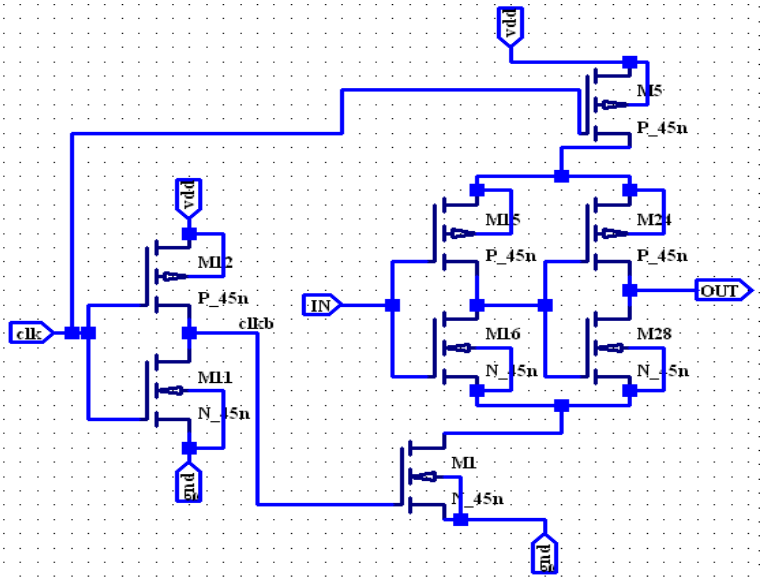

Fig 5: SIS Comparator with Sleep Transistor

Since each comparator is unique in terms of size, the current flowing through each comparator section is also unique, necessitating the usage of a local sleep transistor network rather than a global level one.

3.5. ENCODER

Thermometer code converter

The encoder uses a two-stage process to transform the thermometer's code into binary. The first step is to change the thermometer's code into a one out of n format.

First, a Read only memory (ROM) encoder takes the one out of n codes and converts them into binary code (d2, d1, d0), as illustrated in the below image. A ROM encoder is a common and straightforward tool for converting one-out-of-n codes into binary. A row decoder is used to access the correct row m in the ROM based on the output of comparator m and the inverse of comparator m + 1. If comparator m's output is high and comparator m + 1's output is low, then the row decoder's output m, which is connected to memory row m, will be high. The row decoder can be implemented with a series of 2-input NAND gates with one input inverted. The

fundamental benefit of the ROM decoder method is its easy-to-design regular structure.

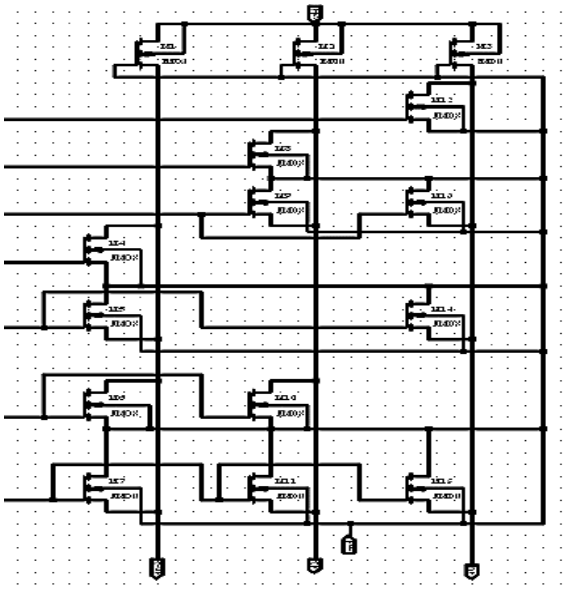

Fig 6: Thermometer ROM Encoder

The output of a thermometer-to-binary encoder is referred to as a thermometer code. This encoder makes primary use of a component that is known as a flash ADC (Analog to Digital Converter). There are a great many effective solutions that have been developed to achieve a more accurate result. One of the most significant issues that arose was the BER, often known as the Bubble error, which is caused mostly by switching noise.

The comparators that make up a Flash ADC will be the primary contributor to the switching noise spreading that occurs. The result is binary, but because to BER, it is corrupted with errors. We would have a good answer if an encoder employed the ROM technique or a combinational circuit that was defined using the Boolean expression. In the field of design, there are a few different effective methods that may be used to extract the thermometer code from an analog value. Let's take it for granted that the code for the thermometer is binary and was stored in ROM or Flash, both of which are fairly efficient storage options.

4. Results

Prior to the development of integrated circuits, engineers had to manually sketch transistors and their connections on paper so that they could be visualized on semiconducting material. This process took a great deal of time. Because larger and more intricate circuits required a significant number of engineers, time, and other resources, there was a desire for a more reliable method of planning integrated circuits within a relatively short period of time.

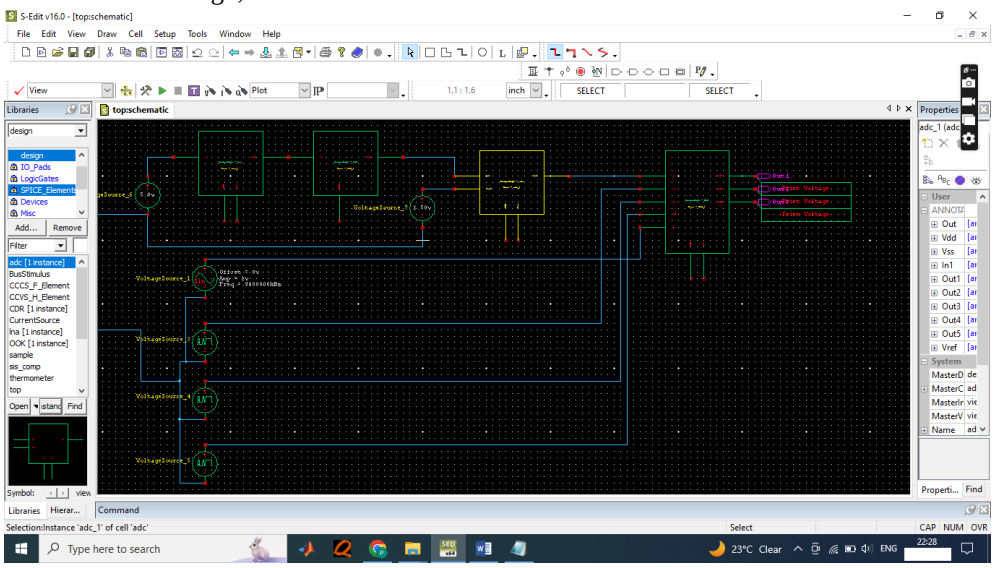

Fig 7: Proposed top level schematic in S-Edit

Utilizing the Tanner EDA tool to draw the schematics. It is necessary to offer some parameters, such as which bit flash ADC is to be constructed, what the (W/L) ratios of PMOS Transistors and NMOS Transistors are, and finally, what the supply voltage that is to be provided for the design is. Using the 45nm technology file, the Tanner EDA program is used to do a simulation of the entirety of the design here. Below, you'll find a discussion of the waveforms and schematic designs associated with a particular schematic. And as a last point of interest, the following also includes a comparison chart that contrasts proposed and existing works in terms of power dissipation and total land area.

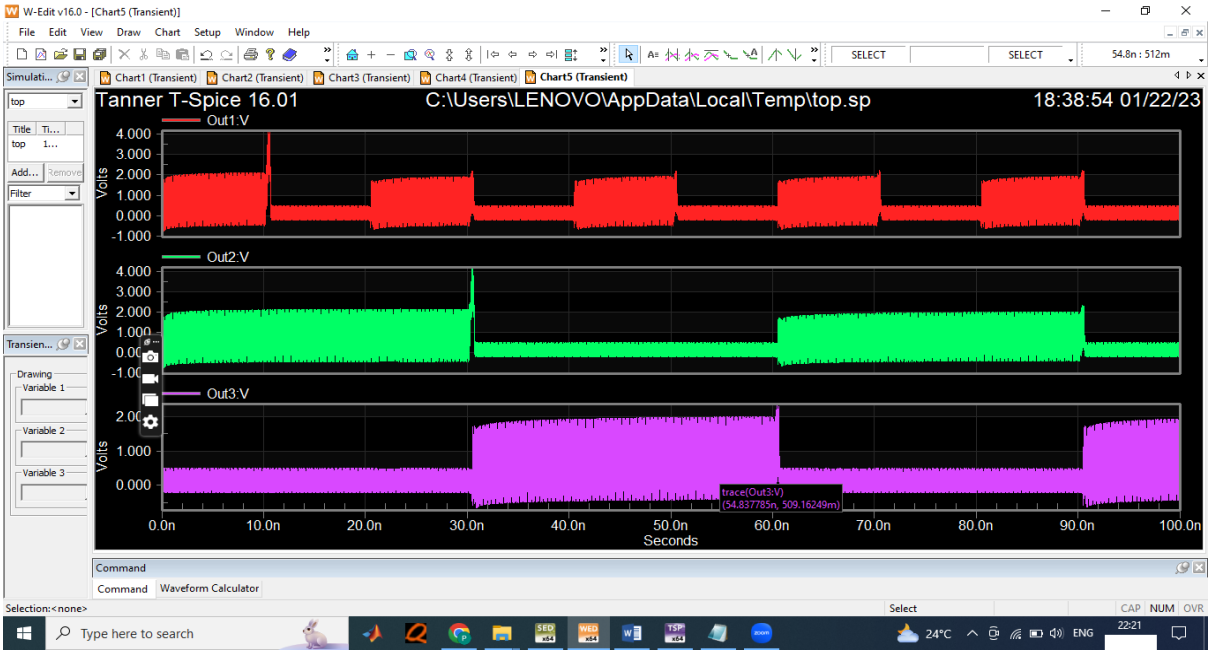

Fig 8: Proposed simulation result for OOK modulation for test case 1

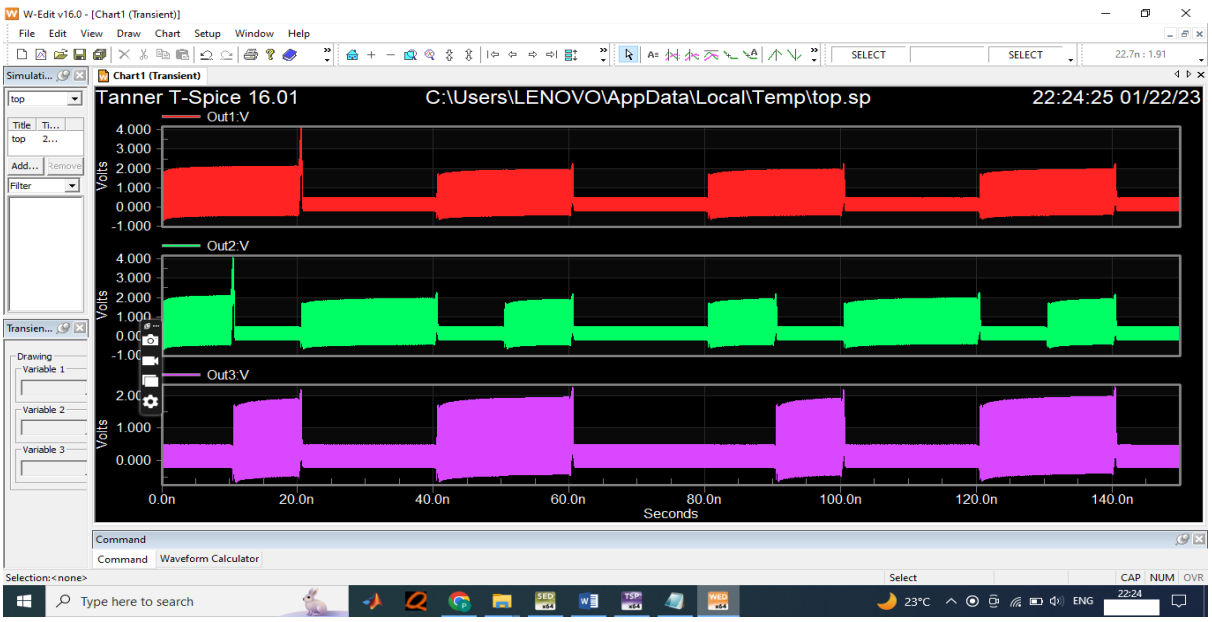

Fig 9: Proposed simulation result for OOK modulation for test case 2

Since we already know this, Area is simply the number of MOSFETs counted. The power that is calculated in Tanner EDA is the average amount of power that is consumed over the duration of the simulation. And the delay that is measured is the difference between the destinations of the particular signals that are specified in the delay command line in terms of when they trigger and when they target.

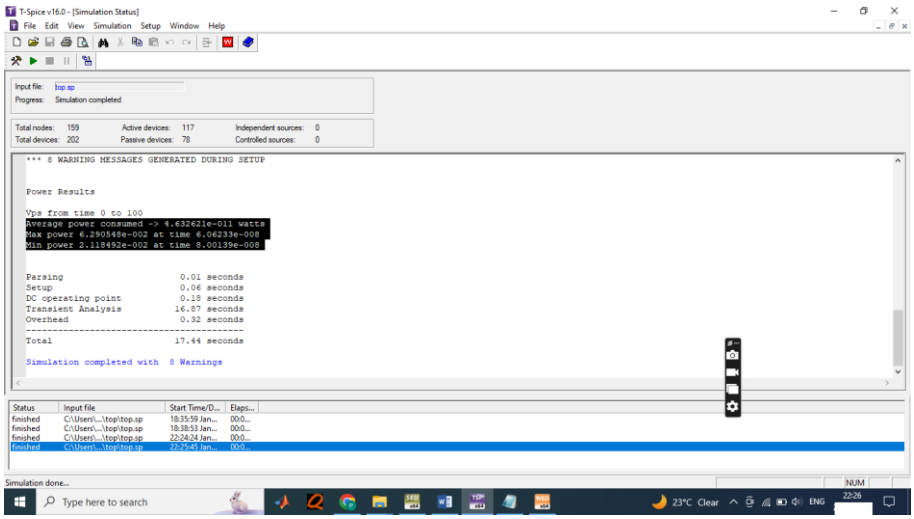

Fig 10: Power consumption report

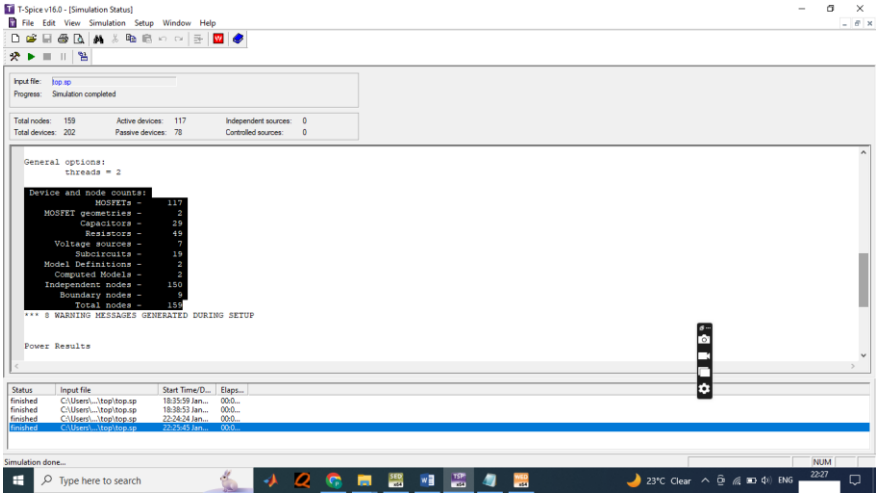

Fig 11: Gate density report

The data presented in the table that is located above reveals that the flash ADC that has been proposed has both less area and lower power dissipation. When compared to other types of flash ADC, the current flash ADC has a smaller region. Figure 12 presents bar graphs illustrating the power consumption of different flash ADC, and Figure 13 depicts bar graphs illustrating the area of distinct flash ADC.

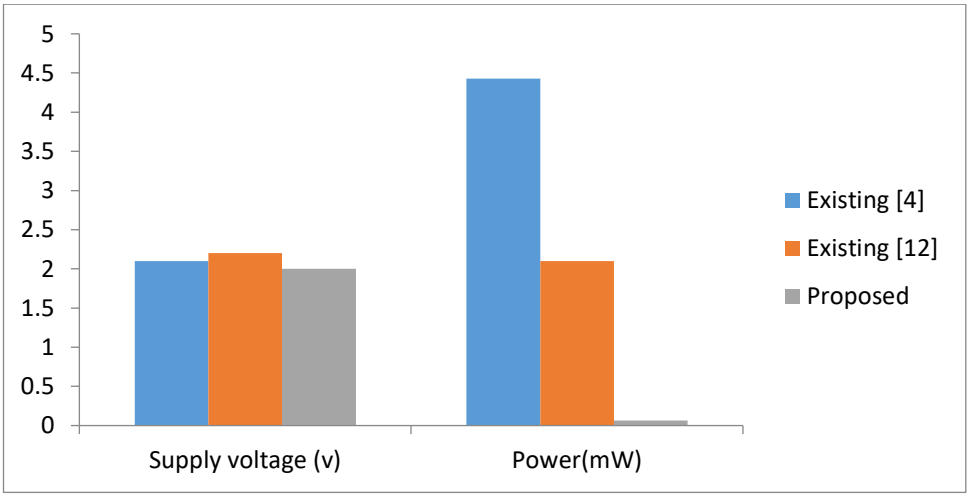

Fig 12: Bar graphs illustrating the power consumption of different flash ADC

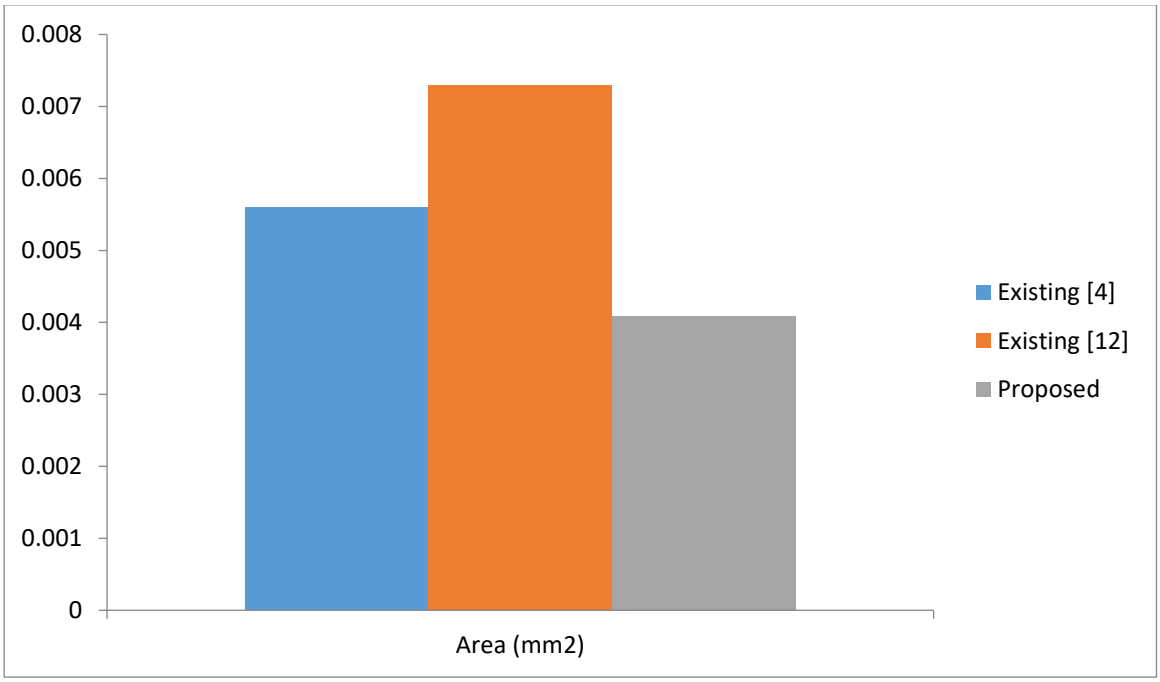

Fig 13: Bar graphs illustrating the area of distinct flash ADC

Table 1: Comparison Table

Parameter	Existing [4]	Existing [12]	Proposed
Supply Voltage	2.1V	2.2V	2V
Area (mm^2)	0.0056	0.0073	0.004086
Power (mW)	4.43	2.1	0.062905

5. Conclusion

In the research, a self-heterodyne CMOS OOK demodulator is proposed. This demodulator would make use of an OMIC LESS SWITCHED INVERTER ADC to process data at Gbps while simultaneously wasting very little DC power. Analytical results have been obtained for the generation of coherent demodulation models for OOK schemes with QN and variable channels. Based on the findings, it is clear that ADC is capable of providing almost optimum performance for the probabilistic detection of OOK schemes across coherent as well as noisy channels. This versatile ADC component has several potential applications, such as capacitive pressure sensors, video systems, low power two-step ADCs, pipelined ADCs, and multi-bit sigma delta ADCs.

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