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Modeling and Performance Analysis of TSV using Nanomaterial-Based Dielectric and Core for High Frequency Applications

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Abstract: Moore's law has been used to increase Integrated Circuit (IC) efficiency over the last four decades by continuously scaling down device geometries. All across the age of precise scaling, IC's have generally used a planar platform. Two new concerns have emerged in recent years. The fundamental one is that device dimension scalability has nearly reached a snag. The second issue is that connection performance is limiting the overall system's effectiveness. The connectivity latency is nearly equivalent to the device delay, making it the true bottleneck. To meet the system's effectiveness requirements, novel interconnect materials as well as creative structures should be created. New integration methods have been developed to minimize interconnect latency. 3D Integration technology is one of the greatest approaches for CMOS applications because it allows multiple layers of devices to be stacked with high-thickness interconnects between them. Aside from that, 3D IC's ability to achieve heterogeneous integration is a big advantage. Noise coupling is a serious issue in three-dimensional IC. As a result, numerous researchers have developed and evaluated alternative materials throughout TSVs and substrates in order to mitigate noise coupling concerns. Three different methods are envisaged: one is the use of various dielectric materials to reduce electrical signal interference when compared to other dielectric materials; the second is the use of three different models such as ETSV, TTSV and heat source to test electrical signal interference on multiple ICs and finally different core materials are proposed to isolate interference. In comparison to previous strategies, the suggested structures and proposed core and dielectric materials produce better results. Furthermore, this paper presents modeling of the signal TSV which is basically useful for high frequency applications.

Keywords: *3D IC; ETSV; Heat source; Noise coupling; Perylene-N; Through Silicon Vias.*

1. Introduction

Within the IC community, noise coupling is the most pressing issue. It's a major worry with 3D ICs, as signals are carried across layers 4 of TSVs, which can cause an electronic storm within the system [1]. The noise is coupled through the TSV into the substrate of each layer, therefore this TSV still builds new barriers. The noise propagates across the substrate, affecting the victim circuits in the vicinity of the TSV [2] – [4]. Noise coupling between TSV-to-Substrate and TSV-to-TSV is a major concern in this design. The volume and direction of the signals propagating in both the aggressive TSV and the victim TSV are dependent on the coupling between TSVs, just like the coupling between interconnections.

Within TSV arrays, the same issue is focused both on capacitive and inductive coupling. To decrease the noise coupled from aggressive TSV to victim TSV, varied manufacturing and design factors are the main goals. In this paper, several approaches for improving noise isolation in 3D IC circuits are proposed.

1.1 Possibilities of using vertical integration in 3D IC

Global interconnects have become a major stumbling hurdle in current VLSI circuits. Because of the parasitic impedance coupled with the long interconnects, the signal quality suffers. The crucial circuits, repeaters, are required to moderate the problems that the global connection is experiencing. By allowing for intimate vertical integration, the 3-D structure will give the greatest answer to this global interconnect problem. Through-Silicon-Via (TSV's) are used to connect devices on nearby levels in 3-D IC structures via short vertical interconnections. These TSVs help to solve global interconnection issues by allowing devices to be tightly integrated in the vertical dimensions [5] – [7]. The primary advantage of employing 3-D ICs is that they have a smaller form factor than 2-D structures. The form factor of a 2-D IC of size A is proportional to A, whereas the form factor of an n-layer 3-D IC of the same area A is proportional to A/n. This capability allows 3-D IC architectures to be used in a compact product. Currently, semiconductor industries not only focuses to increasing the number of devices in a single IC either by novel mechanism, innovative transistor designs [8]–[15] to focus in track with traditional Moore's law but also trying to make it very compact and multi-functional. Also, many researchers have focused on using

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the innovative transistors to apply in various fields like bio-sensing, internet of things, antenna design etc. [16]-[24]. The present work focuses on reduction of electrical signal interference by inserting proper dielectric material as a liner of aggressive TSV and with the different structures like single liner structure (dielectric- Core) and staked liner structure (dielectric-Conducting material-dielectric). Furthermore, noise coupling performance was studied by changing various core materials rather than conventional Copper. Also, this paper focuses on the combination of dielectric along with proper core material, which not only increases the conductivity of signal carrying TSV but also reduces the electrical interference between aggressive TSV (ETSV) and victim TSV. We have chosen a CMOS compatible material for the proposed structures.

1.2 Noise coupling models in 3-D IC

Previously, the work was done on a single block of 3D IC Si substrate. The work is ongoing, with the dielectric materials being changed as an outer layer of TSVs for a single IC block requiring four TSVs [11]. To minimize noise coupling, different dielectric materials are introduced to each TSV's model based on their properties, and the results are studied. The design of a single IC structure is shown in the diagram below. Figure 1 depicts noise coupling model for 3D IC. The model basically has single layer IC where 4 TSV's are accommodated to study the signal integrity, out of four TSV's one is called aggressive TSV which carries electrical signal and other adjacent the TSV is called victim TSV which one is reference to measuring the interference due to signal carrying TSV. The other two opposite TSV's just kept as ground for perfectly analysing the signal interference.

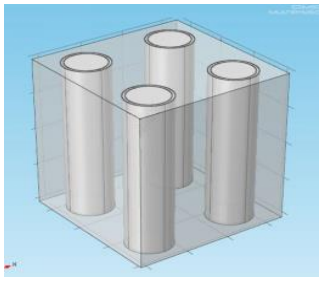

Fig.1: Model of single IC block of 3D IC structure.

Based on Physical configuration a high-frequency salable model has been proposed with resistor, inductor, capacitor, and overall conductance. The aggressive TSV which carries current must have a bump on both the sides of the substrate, the size of the bump is 20 µm as per the standard ITRS road map. Hence, the lumped model is used with frequency up to 10 GHz. The electrical model structure is shown in fig 1. Both aggressive and victim TSV has bumps on the top and bottom. The proposed model uses various parameters which include diameter of TSV (D_{TSV}), bump of one TSV to other TSV pitch (P_{BUMP}), dielectric thickness (T_{ox}), TSV height (h), bump height (H), bump diameter (D).

1.3. Distance between aggressive and victim TSV's

From the aggressive TSV to the victim TSV, the dimensions of 3D IC are measured. TSV that is aggressive is labelled A, whereas a TSV that is victim is labelled B. From point A to point B, i.e., from aggressive TSV to victim TSV, the noise coupling is validated and studied. According to the International Technology Roadmap for Semiconductors, the pitch between two TSVs (the minimal distance between the centres of both neighbouring TSVs) is expected to be 2 um to 8 um (ITRS). The area per TSV is 4 um, with a thickness of 0.15um, a height of 8um, and a thickness of 0.2 um as shown in table 1.

Table 1: Dimensions of (Through-Silicon- Via) TSV as per ITRS Roadmap.

Dimensions of TSV	
TSV's Diameter	2 um
Thickness of Liner	0.2 um
TSV's Height	10 um
Distance between two TSV's	4 um
Pitch between TSV to TSV	2 um

By looking into the above issues in signal integrity from one substrate to another substrate using three-dimensional IC (3D IC) integration is really challenging task. Hence in this study we have proposed a novel electrical model with aggressive TSV carrying electrical signal and isolating by nanomaterial-based dielectric which not only has good dielectric constant but also can be deposited using conventional CMOS process flows.

2. Methodology

There are two different kinds of interface models: an electrical model and a thermal model. Mainly, this work proposes a electrical model. The electrical model also takes into account the skin effect at high frequencies as well as electrical conditions like current jamming and resistivity qualities. Utilizing COMSOL Multiphysics, the evaluation of these interface modes has been approximated. Different dielectric materials and different liner structures were used in the comparison between the two models. To enhance noise isolation, the proposed electrical and thermal models are contrasted. Fig 2 depicts a simulated electrical model using Comsol Multiphysics. Signal integrity and material integrity are the different physics incorporated for the proposed model. For signal integrity we have used electrostatic physics.

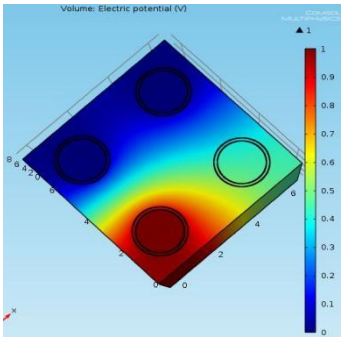

Fig. 2 Electrical model in 3D view.

3. Results and Discussion:

In future IC integration, a new dielectric material with a low dielectric constant (Perylene-N) is used for noise isolation. TSVs are the most significant disadvantage due to inadequate electrical signalling between signal carrier and victim. Noise coupling between TSVs and silicon substrates grows. As a result, a dielectric substance called Perylene-N is employed to reduce noise while consuming less power and taking up less space. The Perylene-N material is compared to conventional SiO_2 material. Prior to the simulation modelling of the through silicon vias is studied through different closed loop equations given below [25] – [30].

$$R_{DC} = \frac{\rho H_{TSV}}{\pi r_{TSV}^2} \quad \text{..... (1)}$$

$$R_{DC} = \frac{\rho H_{TSV}}{\pi(r_1 + H_{TSV} r_2)}\left[1 + \frac{1}{2} r_2^2\right] \quad \text{..... (2)}$$

$$R_{AC} = \frac{\rho H_{TSV}}{\pi(r_{TSV}^2 - (r_{TSV} - \delta)^2)} \quad \text{..... (3)}$$

$$R_{AC} = \frac{\rho(2+r_2^2)}{4\pi r_2 \delta} \ln\left(1 + \frac{2r_2 H_{TSV}}{2r_1 - \delta}\right) \quad \text{..... (4)}$$

$$L = \frac{\mu_0}{4\pi}\left[2H_{TSV} \ln\left(\left(2H_{TSV} + \sqrt{r_{TSV}^2 + (2H_{TSV})^2}\right)/r_{TSV}\right) + r_{TSV} - \sqrt{r_{TSV}^2 + (2H_{TSV})^2}\right] \quad \text{..... (5)}$$

$$L = \frac{\mu_0 R}{2\pi}\left[H_{TSV} \ln\left(\left(H_{TSV} + \sqrt{r_{TSV}^2 + H_{TSV}^2}\right)/r_{TSV}\right) + r_{TSV} - \sqrt{r_{TSV}^2 + H_{TSV}^2} + \frac{H_{TSV}}{4}\right] \quad \text{..... (6)}$$

$$L = \frac{\mu_0}{4\pi}\left[2H_{TSV}\left(\left(H_{TSV} + \sqrt{r_1^2 + H_{TSV}^2}\right)/r_1\right) + 2r_1 - 2\sqrt{r_1^2 + H_{TSV}^2} + 0.5H_{TSV} + \frac{4\beta H_{TSV}(H_{TSV}^2 - (H_{TSV}+r_1)(\sqrt{r_1^2 + H_{TSV}^2} - r_1))}{(\sqrt{r_1^2 + H_{TSV}^2} - H_{TSV})(4r_1 + \beta H_{TSV})}\right] \quad \text{..... (7)}$$

$$L = \frac{\mu_0}{2\pi} H_{TSV} \ln(1 + 2.84 H_{TSV}/\pi r_{TSV}) \quad \text{..... (8)}$$

$$L_{21} = \frac{\mu_0 R}{2\pi}\left[H_{TSV} \ln\left(\left(H_{TSV} + \sqrt{p^2 + H_{TSV}^2}\right)/p\right) + p - \sqrt{p^2 + H_{TSV}^2}\right] \quad \text{..... (9)}$$

RLGC modelling of the TSV is shown in figure 3 where the through silicon vias internal elements and their localities properly modelled. Figure 3 clearly depicts how the lumped- element circuit model and its simplified transmission line model of co-axial TSV are depicted. For modeling we have taken different model parameters like the equivalent capacitance value, equivalent resistance value and equivalent inductance value of a co-axial TSV.

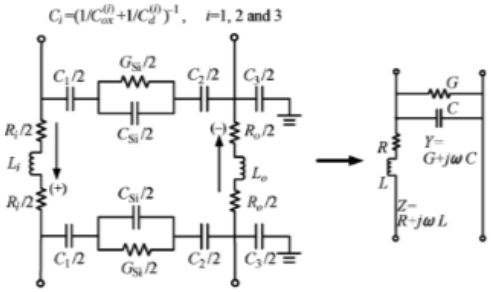

Fig.3 RLCG model of the TSV.

In order to reduce noise in 3D IC integration, various models are applied in numerous ICs. A 3D IC may match together IC chips by stacking them vertically and electrically utilizing TSVs. Coupling of noise is a major problem nowadays for the system performance aspect ratio in 3D integrated circuits using TSVs. TSVs play a crucial role in the electrical signal transmission between 3D ICs and other active devices. Noise coupling between electrical signalling TSV and victim TSV is thus a significant negative. This research demonstrates how altering the dielectric materials for various liner topologies can increase the decrease of noise coupling from TSV to substrate and TSV-to-TSV. Figure 4 shows the top view of proposed electrical model to reduce noise coupling between aggressive TSV (signal carrying TSV) to victim TSV (interfere TSV). Figure 5 shows the simulated noise coupling result from ETSV's to victim TSV. One can clearly observe the reduction in coupling with the use of Perylene-N dielectric material between signal carrying TSV to Silicon substrate up to 30%. Figure 6 clearly depicts the use of Perylene-N dielectric material is comparably better than the conventional SiO_2 liner material.

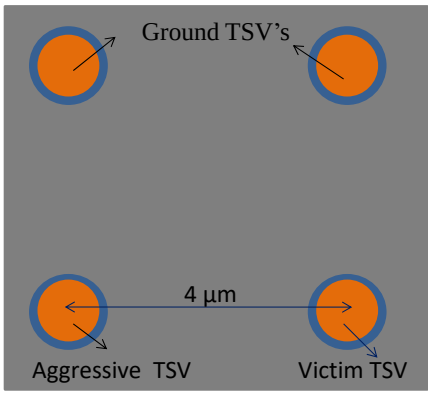

Fig 4: Proposed Noise coupling reduction using Perylene-N material as dielectric.

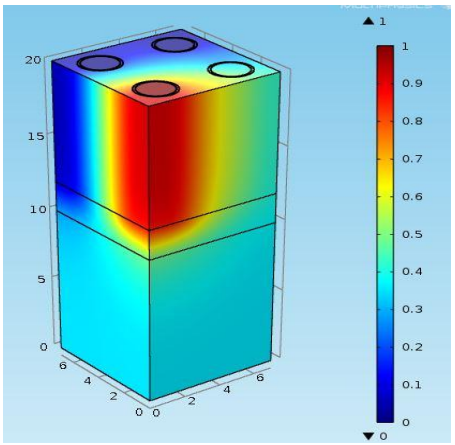

Fig.5 Variations of applied potential between integrated IC's.

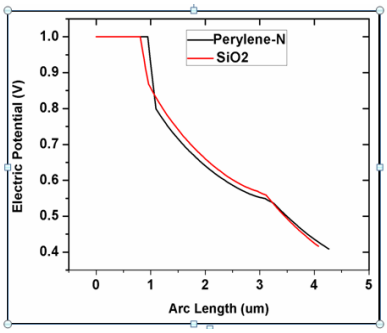

Fig. 6 Differences in applied potential between TSVs made of dielectric materials. Perylene-N and SiO_2 are employed as single liner.

With different core materials and Perylene-N as the dielectric liner material, Figure 7 displays the plot of electrical interference between signal carrying TSV to substrate and signal carrying TSV (ETSV) to victim TSV.

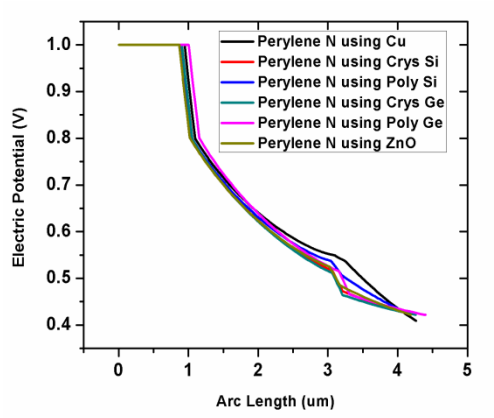

Fig. 7 Variation of Electrical signal from ETSV to Victim TSV with Perylene-N as liner material.

This method reduces the issues with noise coupling in 3D IC integration by applying alternative core materials to the inner layer of TSVs. By separating noise from TSVs to Si substrate, this work demonstrates the superior electrical signal between the layers. Most of the research have up to this point focused on diverse structures, methods, and models, and different dielectric materials are employed for liner constructions, but this work demonstrates with in-depth methodology by utilizing numerous core materials. As core materials, Perylene-N and regular SiO_2 are employed, together with Cu, Crystalline-Germanium, Crystalline-Silicon, Poly-Silicon, Poly-Germanium, and Zinc Oxide nanowires (ZnO). Figure 8 clearly depicts SiO_2 with Crystalline Germanium as a core material inside aggressive TSV reduces noise coupling further compared to other core materials.

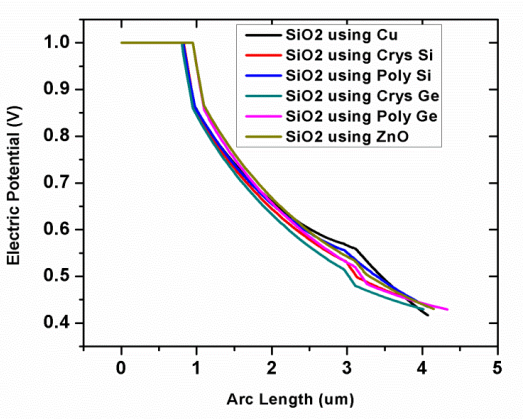

Fig. 8 Variation of noise coupling with different core materials.

Electrical interference was also researched when TSV signals with extremely high frequency ranges up to THz were used. As shown in figure 9, Perylene-N liner material along with Crystalline -Ge has significantly lower interference from signal-carrying TSV to victim TSV than other liner materials simulated with ETSV model.

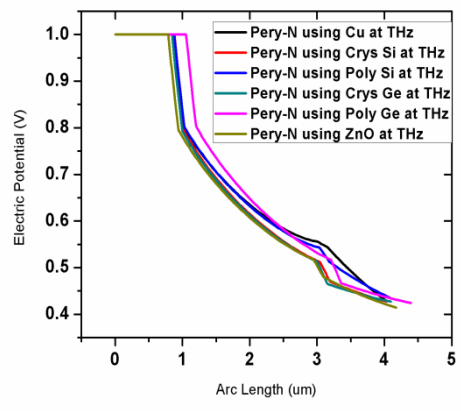

Fig. 9 Electrical Interference study at very high frequency up to 1 THz using different dielectric materials for ETSV model.

4. Conclusion

The goal of scaling and development, which has been practised for decades, is to boost a system's efficiency and usability. It is envisaged that a wide range of emerging technologies, procedures, and materials would coexist in

one system; therefore, 3D-IC is a platform for all of these heterogeneous systems. A number of major obstacles to 3D-IC have been extensively addressed in this thesis, crossing over from all these new devices and creating new approaches to enhance system performance and decrease chip size and area. There have been various theories, approaches, and materials suggested to minimize the noise from TSV to substrate and TSV to TSV. When compared to other dielectric materials, Perylene-N is suggested as a dielectric material to minimize noise. After analysing all the data, the dielectric material (Perylene-N) exhibits enhanced noise coupling performance for single liner and stacked liner. From all of the analysis and results, it is clear that Copper is good for stacked liner structures of both electrical potential mode and high frequency mode, while Crystalline-Germanium is good for single liner structures. Copper also offers excellent electrical signalling by isolating the noise from TSV to Si substrate. In comparison to previous strategies, the suggested structures produce better results. In future, one can integrate to study the temperature effect along with the noise coupling as temperature is also a key factor in Three-Dimensional IC integration.

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Conflict of Interest

The authors declare that they have no conflict of interest regarding the publication of this paper.

Availability of data and material

The data used to support this study are included within the article. No supplementary materials.

Compliance with ethical standards

This article does not contain any studies with human or animal subjects.

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