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Design and Analysis of Low Power VLSI based SRAM Cell using CMOS, FinFET and GNRFET Technologies

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Abstract: Graphene nanoribbon field-effect transistors (GNRFETs) has the ability to be processed and fabricated on a massive scale, making them a viable device for beyond-CMOS nanoelectronics. The primary focus of this study is the design of an SRAM cell using 10 transistors and taking into account two different threshold values. Research efforts centered on FinFET and GNRFET during circuit design. Despite claims of higher performance, lower power consumption, and identical reliability at comparable operating points to scaled CMOS circuits, simulation studies demonstrate that GNRFET circuits are more susceptible to variations and errors. The device and CAD groups working with graphene have some difficult engineering, modeling, and simulation problems to solve as a consequence of these results.

***Keywords*: *CMOS, GNRFET, VLSI, SRAM, HSpice*.**

1. Introduction

Increasing transistor functionality, decreasing power dissipation, and decreasing costs have all been possible thanks to downsizing of semiconductor devices, which has become a driving force in the growth of electronics. In 1965, Intel co-founder Gordon Moore proposed Moore's Law, which states that the number of transistors on a chip will nearly double every two years. With the advent of smaller feature sizes, the semiconductor industry has made enormous gains in recent decades, leading to an increase in the number of transistors per chip. Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) have become crucial to the modern Very Large Scale Industry due to the Moore's Law-driven miniaturization of transistors (VLSI). The size of the MOSFET has decreased from multiple microns to 32 nm or smaller in the last two decades. Short channel effects, drain induced barrier lowering, threshold voltage drop, etc., have begun to affect performance as MOSFET feature sizes continue to shrink. Reduced gate oxide thickness increases leakage current, which slows down the device and increases power consumption. MOSFETs act erratically down in the nanometer region. In recent years, researchers have looked into a wide variety of novel nanotechnology devices, including the field-effect transistor (FinFET), metal-oxide-semiconductor field-effect transistor (MOSFET), carbon nanotube field-effect transistor (CNTFET), graphene nanoribbon field-effect transistor (GNRFET), etc., to address these issues.

Microelectronic memory made of semiconductors are among the most crucial parts of any digital logic system design, including computer-based applications. Large amounts of digital information, necessary for all digital systems, can be stored in semiconductor memory arrays. Storage functions require a larger number of transistors than logic operations or other uses, although the amount of memory needed in a given system is application-specific. Memory and fabrication technologies have advanced in the direction of greater data storage densities to keep up with the ever-increasing need for vast amounts of storage space. The capacity of commercially accessible single-chip read/write memories has reached 1 GB, and on-chip memory arrays are now frequently employed as subsystems in VLSI circuits. Data storage and retrieval methods are the two main categories under which semiconductor memory falls. The bits of information stored in a computer's RAM must be able to be read, written, and accessed whenever necessary (RAM). This data is just for a limited time. SRAM is a great choice for cache memory in microprocessors, mainframes, engineering workstations, and portable devices because of its high speed and low power consumption. Memory cells are often constructed using transistors. Moore's law states, basically, that the total

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number of transistors employed on a single device will grow at an exponential rate. Despite having rapid operating speeds, smaller leakage, and fewer transistors, their efficiency starts to drop below 32nm. The International Technological Roadmap for Semiconductors provides a comprehensive overview of the semiconductor industry's most recent breakthroughs and market trends (ITRS).

New generations of high-performance VLSI devices need for innovative approaches to storing digital information directly on the silicon. The best of these solutions are SRAMs. Many different kinds of microelectronic devices would not function without SRAMS. The increasing pressure from consumers to shrink their electronics has led to this trend. The usage of sub 10nm MOSFETs in very large-scale integrated (VLSI) circuit design is increasingly constrained as a result of issues including susceptibility to process changes and an increase in transistor leakage brought about by scaling. The leakage currents have become a significant obstacle now that scaling has reached a critical apex. These findings call for the development of an entirely new FET system. Graphene's introduction has provided a friendly response to such needs.

Graphene nanoribbon field-effect transistors (GNRFETs) have the ability to be processed and fabricated on a massive scale, making them a viable device for beyond-CMOS nano electronics. Based on atomistic quantum-transport modeling and circuit simulation, experts in the field of GNRFETs have shown that, at equivalent operating conditions, GNRFETs beat scaled CMOS by a factor of over 26-144 in terms of the energy delay product. In addition, the functionality and dependability of GNRFET circuits are analyzed quantitatively in [1], which details the effects of variations and faults. Despite its promise of improved performance, reduced energy consumption, and identical reliability at similar operating points, the simulation results of [1] reveal that GNRFET circuits are more prone to variations and defects than scaled CMOS circuits.

Over the past few years, GNRFETs' theoretical and experimental potential as Low power VLSI circuit design components has been extensively investigated.

Current VLSI circuit designs have a lot of room for improvement with the help of nanoscale devices and Multiple Valued Logic (MVL) [2]. More information could be stored in the same amount of space using MVL based architectures as opposed to traditional binary valued logic design [3]. Ternary computing, also known as three valued logic, has risen to prominence among MVL designs as a result of its ability to minimize chip size and interconnect complexity [4]. Several serial and parallel arithmetic processes can also be performed more quickly by using ternary operations. MVL circuits are typically integrated into ICs that use binary logic to improve performance. It is possible to classify MVL circuits as either current mode or voltage mode depending on the application. Voltage-mode MVL circuits are typically built using multi-threshold CMOS design [4]. The Graphene Nanoribbon Field Effect Transistor is a revolutionary breakthrough in nanotechnology (GNRFET). The key advantages of GNRFETs over CNTFETs are superior scalability and chirality independence. While the cylindrical shape of CNTFETs causes alignment issues, GNRFETs may be produced using a transfer-free, in situ method that is compatible with silicon [5]. Graphene nanoribbons are characterized by their monolayer graphene sheets, small bandgap, and predefined transport channel orientation (GNR). Because of their incorporation of graphene and CNTs, GNRFETs are a novel material with extraordinary electrical characteristics and high mobility. It can carry a lot of current while being relatively cool, and it's thermally stable. Light, strong, switching quickly, and great heat conductor are all qualities they share with graphene [6]. Both metallic and semiconducting GNRFETs are possible due to the presence of a configurable bandgap [7]. Because to its greater mobility and current carrying capability, a GNRFET dissipates less power than FinFET and CNTFET based circuits, according to a performance evaluation report published in [8].

GRAPHENE has recently gained attention as a potential material for beyond-CMOS nanoelectronics due to its unique properties as a monolayer of carbon atoms packed into a 2-D honeycomb lattice. When it comes to electrostatic scaling, monolayer-thin bodies, and carrier velocity for ballistic transport, graphene-based devices excel [9]-[14]. There is great potential for integration with conventional CMOS production methods [14] if graphene sheets can be manufactured on a wafer scale with complete planar processing for devices. This is in stark contrast to the situation with carbon nanotubes (CNTs), which limits production to a few square millimeters at most. Band gaps emerge when field-effect transistor (FET) channels are constructed on graphene nanoribbons (GNRs) only a few nanometers wide [15–18], despite 2-D graphene's status as a zero-band-gap semi-metal. It is necessary to shrink the size of the band gap in a GNR to the sub-10 nm scale, which is an order of magnitude lower than the wavelength of light, so that transistors can function at room temperature. There has been a lot of excitement about the potential use of chemically manufactured sub-10 nm GNRs as transistors because recent samples have shown entirely semiconducting activity [18]. This is in contrast to

CNTs, which are a combination of metallic and semiconducting materials. Arm-chair-edge and zigzag-edge GNRs are the two most common types of GNRs. Both types of GNRs are expected to have hydrogen atoms passivating their edges (AGNRs and ZGNRs). A basic tight-binding model predicts that ZGNRs are metallic, while more complex, spin-unrestricted simulations reveal a band-gap [19]. The use of AGNRs as the channel material in digital circuits has received a lot of attention recently. Similarities exist between the electrical structure of AGNRs and zigzag CNTs. Quantum confinement is responsible for creating the band-gap in AGNRs, with the help of edge effects [19].

Graphene, a monolayer of carbon atoms arranged in a two-dimensional honeycomb lattice, has recently garnered attention as a possible candidate material for next-generation nanoelectronics that extend beyond conventional complementary metal oxide semiconductors (CMOS). Graphene-based devices have great electrostatic scaling, outstanding thermal conductivity, tremendous mobility for ballistic transport, and a monolayer-thin body. Graphene films on a wafer size with full planar processing for devices show greater promise for integration with regular CMOS production techniques than carbon nanotubes (CNTs) [24]. Despite the fact that 2-D graphene is a gapless semimetal, band gaps arise when field-effect transistor (FET) channels are constructed on GNRs of a few nanometers broad [24-27]. For electronic applications, sub-10 nm GNRs are superior to CNTs since they are completely semiconducting due to the edge effect. This was demonstrated in a recent lab study [27].

2. Methodology

1.1 FinFET

One sort of nanoscale technology that can replace conventional complementary metal-oxide-semiconductor (CMOS) technology is the fin-type field-effect transistor (FinFETs). Devices with FinFETs have two gates. A FinFET's performance can be improved by shorting its two gates, while leakage and the number of transistors required can be minimized by controlling the gates separately [28, 29].

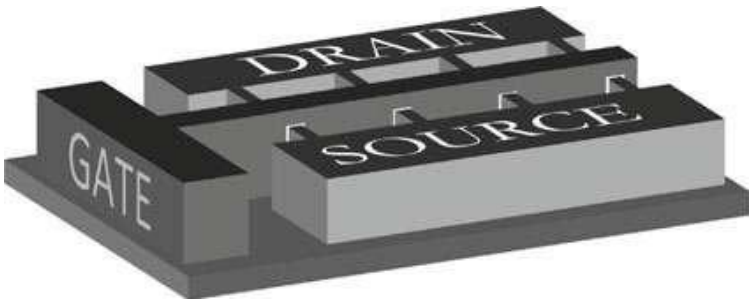


Fig. 1 Multi-fin FinFET

The FinFET chip's gate electrodes surround a wafer-thin silicon core. By relocating the gate electrode to the bottom of the channel, the FinFET enables front and rear gates to be separately controlled. When n is the total number of fins and h is the total height of the fins, the effective gate width of a FinFET is 2nh. Hence, more fins enable wider transistors that can sustain higher on-currents.

1.2 Carbon Nanotubes

Nanotubes made of carbon atoms are cylindrical in shape and exhibit unusually high levels of mechanical, electrical, thermal, optical, and chemical capabilities. Carbon nanotubes come in two different types: Each with one or more walls. Carbon nanotubes (or arrays of them) serve as the channel material in a CNTFET (Carbon Nanotube Field Effect Transistor), rather than the bulk silicon used in a MOSFET. [30-32]

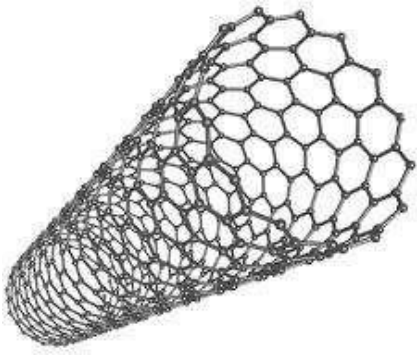


Fig.2 Carbon Nanotube Structure

The nanotubes' folding angle and diameter determine whether they are metallic or semiconductive. Semiconducting nanotubes have a decreasing band gap as their diameter increases. Carbon nanotubes, due to their unique electronic structure, are promising candidates for innovative molecular devices. To get beyond the limitations of CMOS technology, this can be employed even after the 32nm node is reached.

1.3 Graphene Nanoribbon

Graphene nanoribbons, also called nano-graphite ribbons, are very long, very thin sheets of graphene (often thinner than 50 nm). To study the impact of graphene's edges and nanoscale size, Mitsutaka Fujita and co-authors developed the concept of graphene ribbons as a theoretical model. Graphene nanoribbons (GNRs) are the result of a careful patterning process in which graphene is laterally restricted in a ribbon-like form [33–35].

They come in two distinct styles, armchair and zigzag. Each zigzag section has a different angle than the one before it. Each set of two armchair segments is a 120-degree rotation from the set before it. Non-bonding molecular orbitals close to the Fermi energy are transferred from the zigzag edges to the edge localized state. Large shifts in their optical and electrical properties are predicted as a result of their quantization.

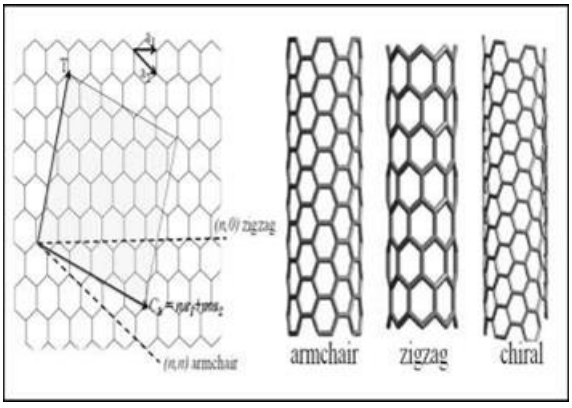


Fig.3 Graphene Nanoribbon

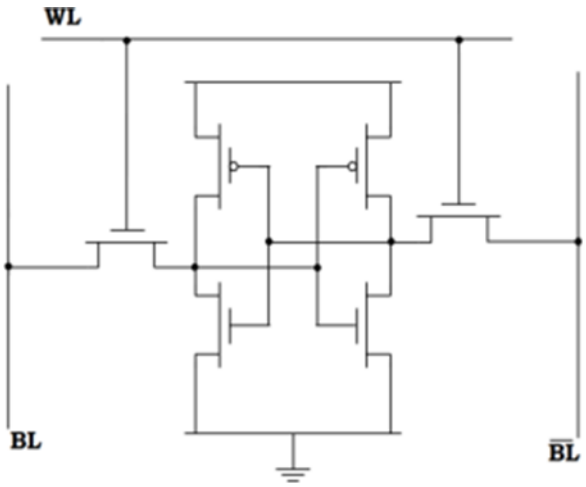


Fig. 4 6T SRAM Cell

1.4 SRAM Cell

SRAM is also known as static random access memory. This technique is commonly used in central processing unit caches, as well as in PCs, workstations, routers, hard disk buffers, and router buffers. Compared to DRAM, which requires regular refreshes, SRAM is superior. Information saved in it is also volatile, meaning it will be lost if the power goes off. Two PMOS transistors and four NMOS transistors are used in the building of a 6T SRAM cell. Using a 6T SRAM cell as a case study, we can better understand how these memory chips work. The functional schematic of a 6T SRAM cell is depicted in Figure 3.

Read, write, and hold are the three distinct modes of operation for SRAM. Bit lines BL and BL' are used in write operations, with the voltage on WL raised and their values set to Vdd or the desired values. The old value of the bit line is completely lost as the new one is written in. When data is present at nodes Q and Q', the WL voltage is raised, prompting memory cells to discharge BL or BL' and allowing the read process to proceed. In the Hold mode, the WL voltage is maintained at a low level while the BLs are either disconnected or driven to Vdd. Every bit in an SRAM is stored in two banks of four cross-coupled transistors. This memory cell may represent the binary digits 0 and 1 with its two stable states. During read and write operations, access to the storage cell is managed by two extra access transistors.

1.5 10T SRAM Cell With Dual Threshold

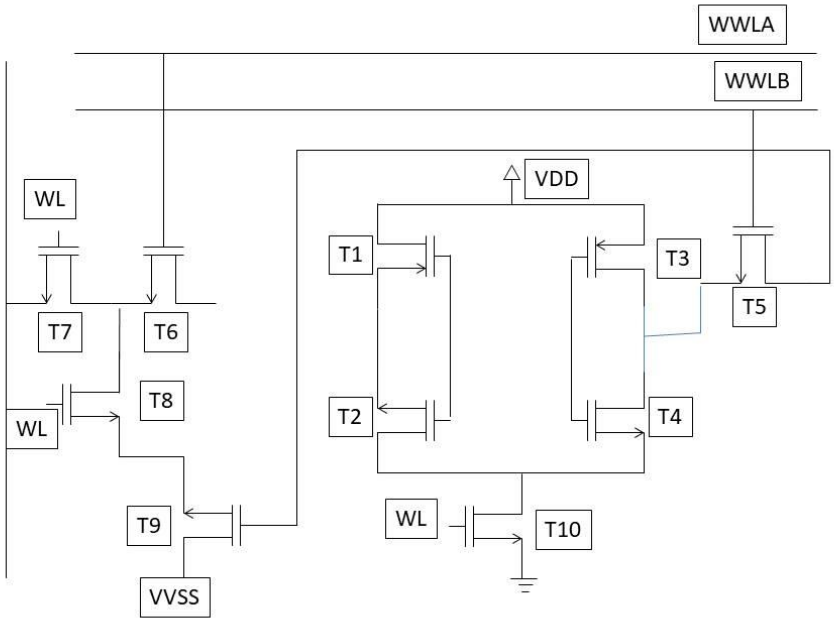


Fig.4 Proposed GNRFET 10T SRAM cell with dual Threshold

Read/write conflicts reduce the performance and reliability of regular 6T SRAM. A dedicated read wordline (RWL) is needed to minimize read interruption in 8T SRAM cells since the write bitline and the read bitline are physically separated. By forcing charges from the bitline into the internal node of the 8T SRAM cell, the write wordline (WWL) causes a half-select problem during interleaving column sharing. As more memory cells were added to the bitline, the half-select issue became more severe. SRAM memory cells that employ a single-ended approach considerably reduce power consumption. It helps minimize the amount of leakage current and the overall size of the chip. Using this single-ended method, the dynamic active can be cut in half. Yet the read/write delays in SRAM cells are more noticeable when the supply voltage is low. Many solutions have been proposed to deal with these issues, including feedback read/write assist, asymmetrical read/write - assist, dual-threshold voltage, cross-point data awareness, and power boost. In this study, we present a novel single-ended GNRFET-based 10T SRAM cell. A sample circuit diagram for a 9T SRAM cell using GNRFETs is shown in Fig. 6. In the suggested cell, data is stored at node Q by means of two cross-coupled inverters, inv1 (T1 and T2), and at node Qn by means of two inverters, inv2 (T3 and T4). The intended 9T SRAM cell can be made more efficient by the addition of a dedicated read/write interface (T5-T9). The new 10T SRAM cell outperforms the 8T SRAM cell by a factor of 2.8 in read disturb immunity with just a 1.2 increase in

area need thanks to its dedicated read port (T7, T8 and T9). SRAM chips' write capacity and cell stability have been enhanced by optimizing the ratio of transistor sizes (T5/T9) in the write port to 1.8. Bit-interleaving is a technique used to improve soft-error rates and reduce coupling-noise levels. Using a high cell count on a single bit line, the row-column select line increases array throughput while decreasing area overhead.

The traditional 6T SRAM cell is an integral aspect of current CMOS-based computer designs and systems. Notwithstanding its shortcomings, such as read/write conflict, half-select disturbance, and read disturb [14], 6T SRAM is a viable component due to its large storage capacity and uncomplicated architecture. Low-voltage instability of conventional Si-CMOS SRAM cells is exacerbated by supply voltage scaling and its effect on performance [15]. Many studies [15-18] have proposed methods for enhancing the stability and performance of low power SRAM design when operating with a low supply voltage. Read buffers that significantly repair the read disturb and obtained read SNM equal to hold SNM [16-18] can improve the read stability of a variety of SRAM cells. Read operations in SRAM cells can be sped up with techniques like suppressed bit lines, negative VSS, and word line under drive, whereas write operations can be sped up with techniques like negative bit lines, word line over drive, and transient voltage collapse [19–21]. Read disturbance is greatly reduced in an asymmetric SRAM cell because of the increased pull-down from a single read port [22]. Although the cell storage node is physically isolated from the read bitline, disturbances can and do occur despite the presence of a feedback mechanism designed to minimize such interference. Leakage current in the subthreshold region is affected by the floating node storage created by the feedback NMOS transistors, which can cause soft errors and multiple cell upset [23]. The effects on several cells can be mitigated by using error checking and repair in a bit interleaving architecture [24]. The standard 6T SRAM cell cannot implement bit interleaving structures due to instability introduced by the selected wordline (WL) execute pseudo read operation [24, 25]. The writeability of both row- and column-based write wordline (WWL) structures is improved by cross-point write architecture's absence of write half-select disturbance; yet, write disturb continues to be a serious issue for both. Hence, this study presents a novel 9T SRAM cell that can operate from a low supply voltage close to the threshold voltage area and is single-ended, disturbance-free GNRFET-based. The suggested cell employs cross-point access to get rid of the write half-select issue, a read buffer to improve read stability, and a single bitline to boost density and cut down on power consumption.

Reducing power consumption while active operation and minimizing leakage current during standby are both made possible by a dual-threshold voltage approach. When comparing cells with different voltage threshold devices, the one with LVT devices has greater SNM than the one with HVT devices. Because of this, selecting a threshold voltage during the production of a high-performance SRAM cell takes only a few seconds [26]. Cells with low threshold voltage devices perform better in noise isolation tests than those with higher threshold voltage devices. The proposed SRAM architecture must employ a supply voltage of less than 0.5V and a technology of no less than 16 nm for a GNRFET with low leakage in order to achieve significant power reductions. The SRAM architecture based on 16 nm low leakage GNRFETs operates optimally at the 325mV supply voltage.

T10 transistors are commonly used to reduce discharge path issues in circuits by driving using the write line. When the write line is on, T10 will turn on. As T10 is unique from the more common 6T and 8T SRAM cells, I plan to focus on that and another topic in this study. To employ a dual threshold method, second.

1.6 Proposed 14T SRAM CELL

Finally, in CMOS development, the standard 6T and 10T SRAM cells are used as the primary storing component and an essential part of PC layouts and architecture. Read/make conflict, the half-select unsettling impact, and read upset are all present in the immediately arranged 6T SRAM with a massive breaking point limit [27]. The standard Si-CMOS SRAM cell's reliability drops precipitously at low stock voltage due to VMIN requirements, which fully corrupts with supply voltage scaling and its display effect [27].

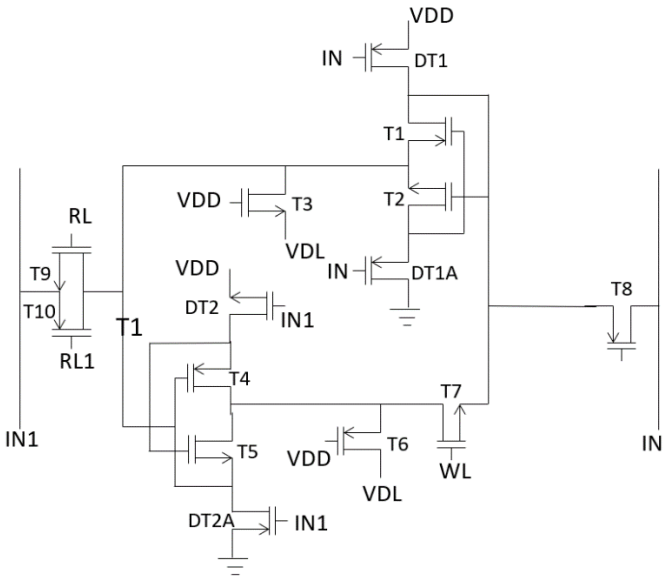


Fig 5 14T SRAM cell with dual Threshold and modified Lector Approach

Typical 6T SRAM cells are used as the primary memory component in the development of CMOS computers. Read/make conflict, the half-select unsettling impact, and read upset are all present in the immediately arranged 6T SRAM with a massive breaking point limit [27]. When the supply voltage is lowered, the reliability of a standard Si-CMOS SRAM cell deteriorates, which in turn affects the exhibit in a negative way because of the VMIN requirements [28]. Some researchers [28-30] have suggested honing one's courage and carrying out a low-force SRAM plan at a low store voltage. Read maintains can be used to strengthen the read security of many SRAM cells, as they effectively update the read steamed to make read SNM indistinguishable from hold SNM [29-31]. Strength of pull down to pass entrance and surrender entrance to pull, freely, are refreshed; covered digit line, negative-VSS, and word-line-under-drive are utilized to enhance read tasks; negative-cycle line, word-line-over-drive, and transient-voltage-breakdown are utilized to enhance make tasks; and isolating is utilized to enhance make tasks. When it comes to read security, a disproportionate SRAM cell's single read port and increasing pull-down strength are key factors in reducing read upset [35]. Read upset persists despite efforts to mitigate it via the information system, which have yielded a fundamental improvement in consistency via the limitation of telephone collection efforts with respect to read bitline. Gliding focal point storage is activated by the NMOS semiconductors used in the study, which influences spilling current in the subthreshold region and may, in turn, initiate delicate mess up and varied cell upset [36]. Using the piece interleaving strategy with fumble check and adjustment [37], you may limit the disruption to the various cells. Picked wordline (WL) conduct pseudo read development drains power, making the typical 6T SRAM cell inappropriate for digit interleaving architecture [38, 39]. When applied to both line and segment based structures, wordline (WL) planning eliminates the make half-select uncomfortable affect that reduces writeability. As a result, this study proposes a novel FinFET-based 14T SRAM cell that operates at low stock voltage close to the restrict voltage area and features a single-finished marvel-free design. The proposed cell gets rid of the make half-select issue and increases thickness while decreasing power consumption by using read cushion and cross-point access, respectively. Using a double-limit voltage technique, which also aids in reducing leakage current in the dormant phase, can assist minimize the power consumption of an activity-based approach. The cell's SNM is greater when equipped with low voltage limit (LVT) devices than when equipped with high voltage edge (HVT) devices. As a result, a typical SRAM cell's choice-averse voltage decision can be made quickly through efficient organization [40, 41]. The resistance to disturbing influences is significantly stronger in the cell with low-limit voltage devices than in the cell with high-edge voltage. To improve power efficiency in the proposed SRAM scheme, it is essential to settle on a stock voltage of the gadget lower than 0.5V, and to move forward with 16 nm low spillage FinFET technology. For the sake of practicality, the stock voltage of the 16 nm low leakage FinFET-based SRAM architecture has been lowered to 325 mV. T10 semiconductors are widely used because they drive with manufacture line, which helps to reduce the circuit's conveyance way problem. When the make line is ready, T10 will turn on automatically. I need to zero in on T10, which has been shown to work for standard 6T and 8T SRAM cells, and another variable in this analysis. As a second, employ a framework with two edges. Read/make conflicts weaken the effectiveness and attractiveness of the industry

standard 6T SRAM. In an 8T SRAM cell, the make bitline and the read bitline are physically separated to lower the read upset. This separation makes use of a separate read line (WL). Half-select problems occur in the interleaving region when charges are transferred directly from the bitline to the 8T SRAM cell's internal focus, and this is where the structure line (WL) comes into play. The half-select issue became more bothersome as the bitline's capacity for memory cells increased. Using a specific finished method significantly reduces force spread in SRAM memory cells. Both the leakage current and the chip pattern area are drastically decreased. With this streamlined strategy, we can reduce the remarkable dynamic by one component. In any case, the degree of inspection/structure delays at the low stock voltage distorts the SRAM cell's familiarity. Exam read/make help, unequal read/structure - help, double edge voltage, cross-point-information cautious, and force support are just few of the unmistakable analyze and make aid solutions presented to overcome these challenges. Here, we present an innovative 14T SRAM cell that employs completed FinFETs in a single step. Using FinFETs, Fig. depicts the design of a typical 14T SRAM cell. Two cross-coupled inverters, inv1 (T1 and T2) and inv2 (T3 and T4), hold data on the focus Q and Qn (T5 and T4). The suggested 9T SRAM cell's display capabilities could be improved by adding a second read/structure port (T5-T9). Taking taking account the restricted read port, the new 14T SRAM cell has a computed miracle impediment that is 2.8 times higher than that of an 8T SRAM cell of equal area overhead (T7, T8 and T9). In order to get the most development and power out of each SRAM cell, the semiconductors' assessment degree (T5/T9) of the structure port has been increased to 1.8. In order to reduce coupling complaints and clean up the sensitive mess, the pieces will be interleaved. In order to increase bunch capacity while decreasing region overhead, the enormous cell count on the select line is put to use.

LECTOR APPROACH

A new method, LECTOR (Fig. 6), was proposed by Narender Hanchate et al. for minimizing leakage power in CMOS circuits. It utilized a PMOS and an NMOS leakage control transistor (LCT) within the logic gate. Each LCT's source regulates the LCT's gate terminal. For every given set of inputs, one of the LCTs will be very close to its breakdown voltage in this configuration. This dramatically reduces leakage currents by increasing the resistance on the path from Vdd to ground. This technique outperforms others in terms of minimizing leakage in both the on and off states of a circuit. The experiments show that the leakage in the MCNC reference circuits is reduced by an average of 79.4 percent.

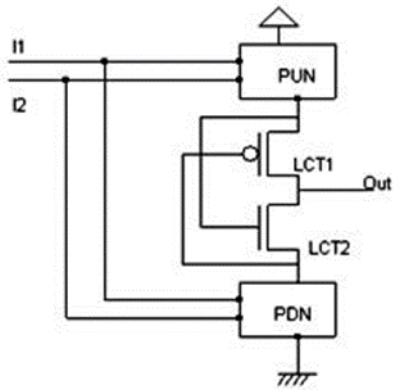


Fig 6: LECTOR technique

SRAM is also known as static random access memory. This technique is commonly used in central processing unit caches, as well as in PCs, workstations, routers, hard disk buffers, and router buffers. Compared to DRAM, which requires regular refreshes, SRAM is superior. Information saved in it is also volatile, meaning it will be lost if the power goes off. A 6T SRAM cell is constructed using two PMOS transistors and four NMOS transistors. To learn more about how these memory chips function, we'll use a 6T SRAM cell as an example. A functional schematic of a 6T SRAM cell is depicted in Figure 3. SRAM can be used in three different modes: read, write, and hold. Bit lines BL and BL' are used in write operations, with the voltage on WL raised and their values set to Vdd or the desired values. The old value of the bit line is completely lost as the new one is written in. When data is present at nodes Q and Q', the WL voltage is raised, prompting memory cells to discharge BL or BL' and allowing the read process to proceed. In the Hold mode, the WL voltage is maintained at a low level while the BLs are either disconnected or driven to Vdd. Every bit in an SRAM is stored in two banks of four cross-coupled transistors. This memory cell may represent the binary digits 0 and 1 with its two stable states. During read and write operations, access to the storage cell is managed by two extra access transistors.

Here, we provide a high-level summary of the models employed to calculate short-channel FETs' power dissipation. In this device, the drain current is highly nonlinear with respect to the source and drain voltages, making it difficult to calculate the leakage current. To determine the amount of energy that was wasted as a result of leakage, we employed the Berkeley Short-Channel IGFET (BSIM) Predictive Technology Model, which is in good agreement with HSPICE simulations [42,43]. The threshold voltage is assumed to be based on the BSIM model, which is

$$V_t = V_{FB} + \phi_s + k_1\sqrt{\phi_s} - k_2\phi_s - \eta V_d$$

The drain-induced barrier lowering (DIBL) effect models the flow of an unwanted punch-through current between the source and drain below the surface of the channel, where VFB is the flat band voltage and k1 is the Fermi potential and a reflection of the effect of nonuniform doping. Current leakage in poorly inverted NMOS transistors

$$I_s = I_0 \exp\left(\frac{(V_{gs} - V_t)}{nV_T}\right)\left(1 - \exp\left(-\frac{V_{ds}}{V_T}\right)\right)$$

3. Simulation Results

Graphene nanoribbon field effect transistors (GNRFETs) are an exciting development in the realm of nanoelectronics. Since GNRFETs are scalable and free of the chirality issues that plague CNTFETs, they are the superior technology. Non-alignment and similar issues with CNTFETs, which have a cylinder form, are eliminated through the use of transfer-free, in situ GNRFET development that is compatible with silicon. Monolayer graphene sheets with a narrow bandgap can be arranged in a specific transport channel orientation to create graphene nanoribbons (GNR). The unique electrical properties and high mobility of GNRFETs are the result of the material adopting the properties of both graphene and CNTs. It can carry a lot of current while being relatively cool and producing little heat. Graphene has excellent switching properties and is a good heat conductor. The bandgap of GNRFETs can be adjusted, allowing them to take on either a metallic or semiconducting state. Based on its increased mobility and current carrying capability, a GNRFET dissipates less power than FinFET and CNTFET based designs, according to a performance evaluation research published in [1].

A novel type of graphene-based nanoelectronics called graphene nanoribbon field effect transistors (GNRFETs) shows great promise. The scalability and lack of chirality issues that characterize GNRFETs make them the preferred choice over CNTFETs. The growth of GNRFETs is made possible via a transfer-free, in-situ method that is compatible with silicon, hence eliminating the need for alignment and other issues.

connectable to CNTFETs. The transport channel orientation of graphene nanoribbons (GNR) is engineered to take advantage of the material's tiny bandgap. Combining the best of graphene and carbon nanotubes (CNTs), GNRFETs become a new material with exceptional conductivity and mobility. It can carry a lot of current without getting too hot, and it's also thermally stable.

They're easy to transport, powerful, switch quickly, and great at transferring heat. GNRFETs can be either metallic or semiconducting due to the presence of a configurable bandgap that allows them to assume this behavior. In comparison to FinFET and CNTFET based devices, GNRFET's superior mobility and current carrying capability result in lower energy usage, as stated in [1].

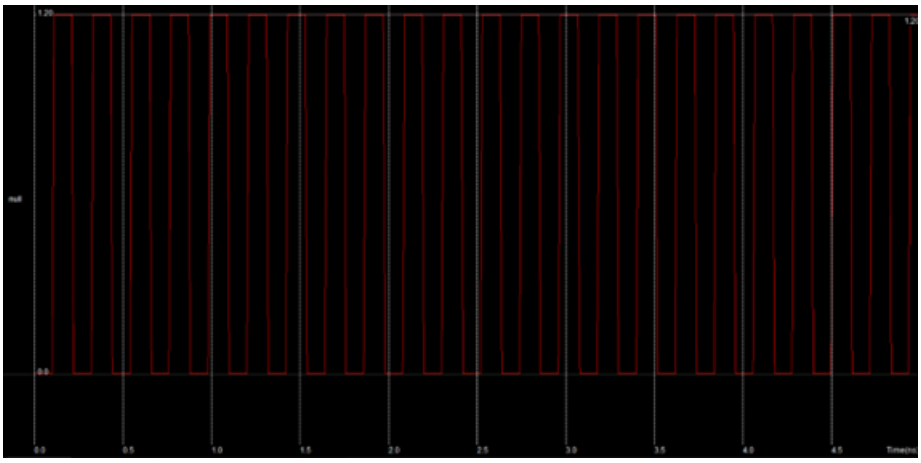


Fig 5 (a)Timing Diagram

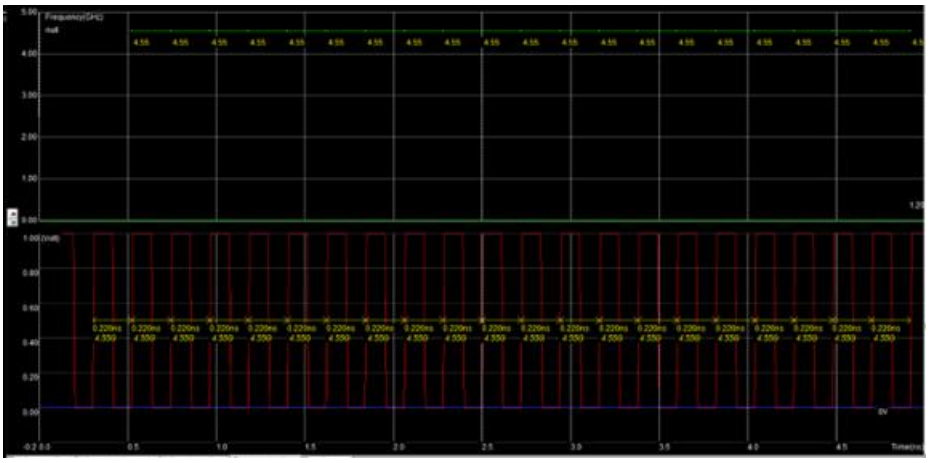


Fig 5 (b) Timing Diagram

Table 1: Comparison with FinFET and CMOS of 14T SRAM Cell 1 bit

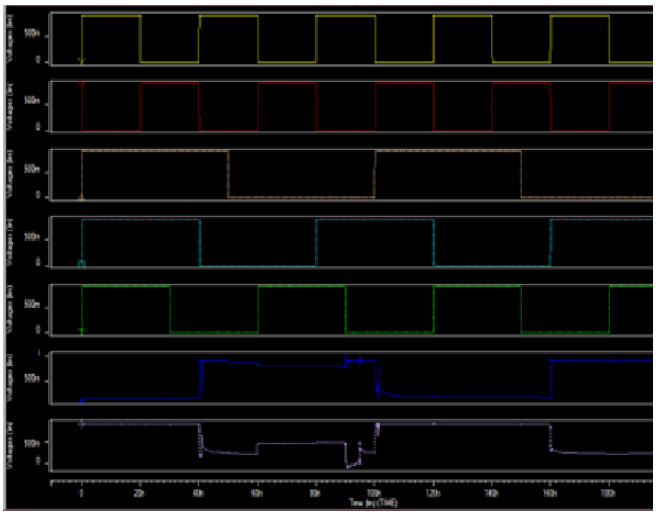
S.NO.	NM	Power in mW for CMOS	Power in mW for FinFET	Power in nW for GNRFET
1	22	6.08	3.57	2.49
2	14	5.32	3.28	-
3	10	5.76	2.67	-
4	7	5.68	2.53	-

Table 2: Comparison with FinFET and CMOS of 14T SRAM Cell 4 bit

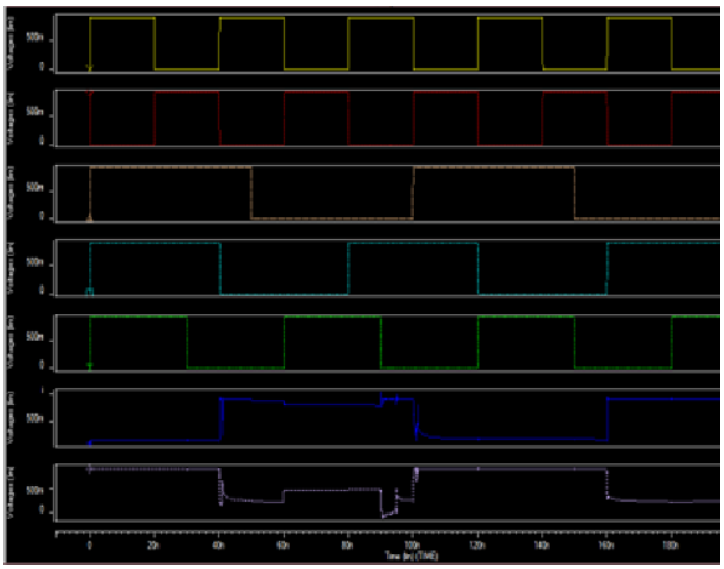
S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET	Power in nW for GNRFET
1	22	2.81	1.35	1.17
2	14	2.36	1.26	-
3	10	1.92	1.22	-
4	7	1.82	1.19	-

Table 3: Comparison with FinFET and CMOS of 14T SRAM Cell 8 bit

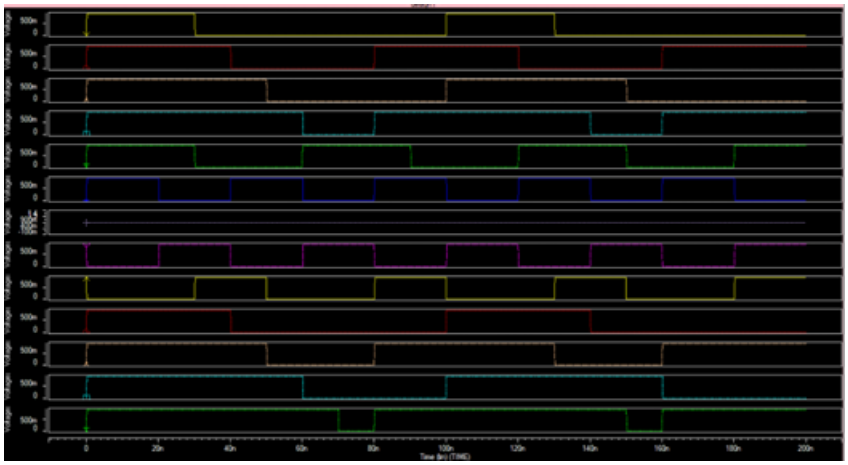
S.NO.	NM	Power in nW for CMOS	Power in nW for FinFET	Power in nW for GNRFET
1	22	3.01	1.92	1.46
2	14	2.62	1.72	-
3	10	2.21	1.65	-
4	7	1.98	1.58	-



(a)



(b)



(C)

Figure 5 Wave forms for (a) 1 bit (b) 4 bit (c) 8 bit

Table 4 Technology Parameters 22nm-1bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	3.5702E-05 from= 0.0000E+00 to= 2.0000E-07
2	Avgpwr	3.5989E-05 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	Failed
4	Trig	not found
5	Tpd	2.7406E-11
6	qn_rise_delay	2.7406E-11
7	qn_fall_delay	-2.9433E-11
8	SupplyCurrent	1.5602E-05 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-7.8011E-06
10	high_low_total_energy	3.8728E-14
11	low_to_high_total_energy	3.9283E-14
12	dynamic_energy	7.8011E-14
13	total_dynamic_energy	3.9005E-14
14	total_dynamic_power	-1.2346E-29

Table 6 Technology Parameters 22nm-4 bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.3515E-09 from= 0.0000E+00 to= 2.0000E-08
2	Avgpwr	1.3515E-09
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	1.8714E-10
7	qn_fall_delay	3.8400E-11
8	SupplyCurrent	6.5328E-10
9	Static power	5.8795E-10
10	high_low_total_energy	5.8867E-18
11	low_to_high_total_energy	7.2297E-21
12	dynamic_energy	5.8795E-18
13	total_dynamic_energy	2.9398E-18
14	total_dynamic_power	1.2346E-29

Table 6 Technology Parameters 22nm-8 bit FinFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.9230E-09 from= 0.0000E+00 to= 3.0000E-08
2	Avgpwr	1.9230E-09

3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	2.1673E-11
5	Tpd	2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11
8	SupplyCurrent	1.3066E-09
9	Static power	-1.1759E-09
10	high_low_total_energy	1.1773E-17
11	low_to_high_total_energy	-1.4459E-20
12	dynamic_energy	1.1759E-17
13	total_dynamic_energy	5.8795E-18
14	total_dynamic_power	-1.2346E-29

Table 4 Technology Parameters 22nm-1bit GNRFET

S.NO.	**PARAMETER**	**VALUE**
1	Power_avg	2.4929E-08 from= 0.0000E+00 to= 2.0000E-07
2	Avgpwr	5.8509E-08 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.0215E-08 targ= 4.0260E-08 trig= 4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11 pdp= 0.0000E+00
8	Supply Current	1.6332E-10 from= 0.0000E+00 to= 1.0000E-08 staticpower= -1.4699E-10
9	Static power	-1.6748E-01
10	high_low_total_energy	1.6352E-18 from= 0.0000E+00 to= 5.0000E-09
11	low_to_high_total_energy	-1.8074E-21
12	dynamic_energy	1.4699E-18
13	total_dynamic_energy	7.3494E-19
14	total_dynamic_power	-1.2346E-29

Table 6 Technology Parameters 22nm-4 bit GNRFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.1715E-09 from= 0.0000E+00 to= 2.0000E-08
2	Avgpwr	5.8509E-08 from= 5.0000E-09 to= 2.0000E-07
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11
8	SupplyCurrent	6.5328E-10 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-5.8795E-10
10	high_low_total_energy	5.8867E-18
11	low_to_high_total_energy	-7.2297E-21
12	dynamic_energy	5.8795E-18
13	total_dynamic_energy	2.9398E-18
14	total_dynamic_power	-1.2346E-29

Table 6 Technology Parameters 22nm-8 bit GNRFET

S.NO.	PARAMETER	VALUE
1	Power_avg	1.4630E-09 from= 0.0000E+00 to= 3.0000E-08
2	Avgpwr	1.6797E-10 from= 5.0000E-09 to= 3.0000E-08
3	q_rise_delay	3.6266E-11 targ= 8.0944E-11 trig= 4.4678E-11
4	Trig	4.4678E-11
5	Tpd	0.0000E+00 targ= 2.1673E-11 trig= 2.1673E-11
6	qn_rise_delay	-1.8714E-10 targ= 2.1673E-11 trig= 2.0881E-10
7	qn_fall_delay	3.8400E-11 targ= 8.2810E-11 trig= 4.4410E-11 pdp= 0.0000E+00
8	SupplyCurrent	1.3066E-09 from= 0.0000E+00 to= 1.0000E-08
9	Static power	-1.1759E-09
10	high_low_total_energy	1.1773E-17
11	low_to_high_total_energy	-1.4459E-20
12	dynamic_energy	1.1759E-17
13	total_dynamic_energy	5.8795E-18
14	total_dynamic_power	-1.2346E-29

4. Conclusion

Traditional Si-CMOS technology is struggling to keep up with the demands of ever-smaller devices because to difficulties such short channel effects, higher leakage current, and process variance [35, 36]. Conventional Si-CMOS technology suffers strain as a result of modern manufacturing techniques, and its scalability is constrained by short channel effects. FinFET, silicon-on-insulator (SOI) MOSFET, and carbon-based devices have largely supplanted conventional CMOS in recent years [38–40]. Carbon nanotube field effect transistors (CNTFETs) and graphene nanoribbon field effect transistors (GNRFETs) stand out as prospective alternatives due to their remarkable electrical characteristics and high-density capabilities, made feasible by breakthroughs in fabrication techniques. There are problems with alignment and transfer in CNTFET-based devices, but they are avoided in GNRFET-based devices [36]. Higher metal-contact resistance causes more heat to be dissipated, which is another problem with CNTFET technology. Transfer-

free fabrication is an easy in situ procedure that is silicon compatible and may be used to create GNRFETs [37]. Heat dissipation, delays, and power consumption are all drastically reduced in GNRFETs compared to traditional Si-CMOS and CNTFET based devices because of their low metal-contact resistance [38]. As metal-low graphene has low contact resistance, it can be used in high-speed electronic devices and is hence a potential component in high-speed memory circuits. However, advancement is hindered by the fact that graphene-based transistors have an unstable conductivity as a result of manufacturing changes and a zero bandgap [39, 40]. To ensure that graphene nanoribbon FET memory circuits can function in practical contexts, it is necessary to assess these effects.

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