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Power-Efficient Reconfigurable FRM Filter-Bank using Brent Kung Adder for Hearing Aids

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Abstract: Efficient power usage is a key design criterion for hearing aids as they are battery-powered devices. Low power consumption of hearing aid leads to longer battery life, and smaller and lighter battery without compromising the operation time and improving the convenience and overall satisfaction of hearing impaired. To further improvise the user experience and comfort, filter banks which are reconfigurable in nature are used in hearing aids making them more customized and flexible to varying hearing profiles of patients. Thus, reconfigurability with efficient power utilization is the key filterbank requirement in hearing aid. The paper presents a design of a power-efficient reconfigurable Frequency Response Masking(FRM) Filter bank for hearing aid. The Distributed arithmetic technique is employed to generate distributed RAM partial product generators which are then accumulated using adders. For fast and power-efficient operation, Parallel Prefix Adder (PPA) is chosen against sequential adders. In this paper, four types of PPA viz. Kogge-Stone Adder (KSA), Brent Kung Adder (BKA), Han-Carlson Adder (HCA) and Ladner-Fischer Adder (LFA) are designed and compared for their power and resource utilization. Further, filter banks are designed using all four adders as part of their processing unit using Verilog HDL in Xilinx Vivado 2018 and implemented in Kintex 7 FPGA Genesys 2 board. Experimental results confirm that the reconfigurable filter bank designed using Brent Kung adder has the least power requirement amongst all four PPA-based filter designs and consumes 39.74% lesser power compared to the existing reconfigurable filter design using Carry Bypass adder.

Keywords: *Distributed Arithmetic, FPGA, Frequency Response Masking, Han-Carlson Adder, Kogg-Stone Adder, Ladner-Fischer Adder, Parallel Prefix Adders*

1. Introduction

Hearing is essential to communicate effectively with others and interact with the world around them. Hearing is a crucial sense that enables individuals to participate fully in social, educational, and occupational activities. A hearing problem leads to difficulty in hearing sounds or speech. Hearing impairment is also associated with daily-life fatigue since reduced audibility lead to increased listening exertion to maintain performance. [1] Hearing problems can range from mild to severe and can be caused by various factors such as aging, exposure to loud noise, genetic factors, infections, trauma, and certain medical conditions. Sensory-Neural hearing loss(SNHL) is the problem in the nerve pathways that transmits sound from the inner ear to the brain resulting in impaired speech discrimination and recognition[2]. This hearing problem should be addressed at the earliest since prolonging may cause social isolation, depression, and other negative outcomes. Hearing Aids can help the hearing impaired regain their hearing ability by picking up, processing and amplifying the sounds which the HI is unable to hear. They achieve improve speech intelligibility and listening comfort through the use of various hearing aid algorithms and appropriate HA programming with the help of an audiologist.[3] A filter bank is a critical component of a hearing aid that helps to process and amplify specific frequency ranges of sounds that a person with hearing loss may struggle to hear. The filter bank in a hearing aid is typically made up of multiple digital filters that are designed to separate incoming sounds into individual frequency bands, allowing for more precise and targeted amplification[4]. In a filterbank system for a hearing aid, the analysis and synthesis blocks divide input audio in multiple sub-bands and then combining them back together, respectively as shown in Figure 1.

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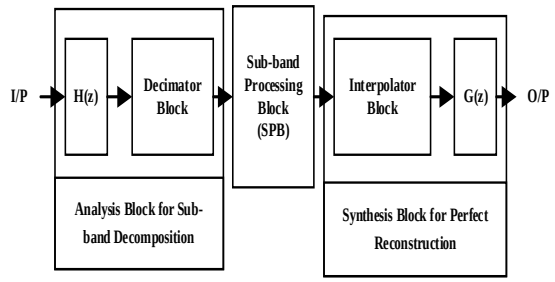

Fig 1. Structure of generic filter bank

Decimation or down sampling is a process of reducing signal sampling rate by decimation factor (M). The decimation processing can be represented by equation (1) in the frequency domain.

$$Y(z) = \frac{1}{M}\sum_{k=0}^{M-1} X\left(z^{\frac{1}{M}} W_M^k\right) \quad (1)$$

Interpolation or up sampling is process to increase signal sampling rate by interpolation factor (L). Equation (2) represents the interpolation process in the frequency domain.

$$Xu(z) = X(zL) \quad (2)$$

The reconfigurable filter bank can be dynamically adjusted to meet the changing listening needs of the wearer improving their speech intelligibility and sound quality in noisy environments, as well as greater flexibility and customization of the hearing aid's performance[5]. The Processing Unit (PU) of the filter bank comprises of Distributed RAM Partial Product Generator (PPG) and Shift Accumulator as shown in Figure 2.

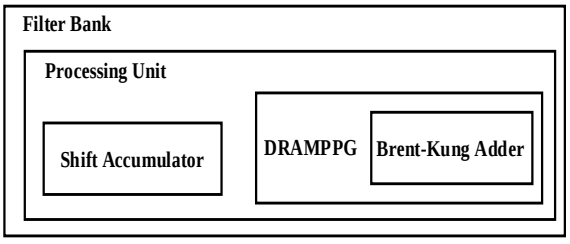

Fig 2. Structure of processing unit module of filter bank

Distributed RAM PPG is used to efficiently produce the partial products needed for multiplication operations involved in filtering process. These partial products are then accumulated using adders. The adders *perform t*he necessary summation operations to combine the partial products and produce the final filterbank output.

For hearing aid applications, various adders can be utilized for filter bank design viz. RCA, CLA, CSLA and PPA[6]. PPA generates the carry graph using a parallel approach[7]. This allows the sum bits to be computed simultaneously, reducing the carry propagation delay and allowing for faster addition compared to sequential adders. PPA structure comprises of Processing block, carry graph generation block and post processing block as shown in Figure 3.

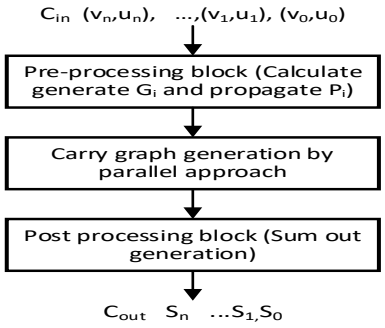

Fig 3. Working model of Parallel Prefix Adder

STAGE I: In Preprocessing block, propagate signal Pr and Generate signal Gn are calculated as given by equations (3) and (4) respectively.

$$Pr[i] = u[i] \oplus v[i] \quad (3)$$

$$Gn[i] = u[i] \bullet v[i] \quad (4)$$

Where u and v are the input signals.

STAGE II: In carry-signal generation stage, precomputed Pi and Gi values are taken into consideration and Carry-propagate (Pcarry) and Carry-generate (Gcarry) signals are calculated as depicted by equations (5) and (6) respectively.

$$Pcarry = Pr[i] \bullet Pr[i+1] \quad (5)$$

$$Gcarry = (Gn[i] \bullet Pr[i+1]) + Gn[i+1] \quad (6)$$

STAGE III: In post processing block, the output signals and final result of the adder sum and carry out is generated using the carry values computed in previous stage using equation (7) and (8) respectively.

$$S[i+1] = Pr[i+1] \oplus C[i] \quad (7)$$

$$C[i+1] = (Pr[i+1] \bullet Cin) + Gn[i] \quad (8)$$

Where C is carry signal of previous stage and Pr is propagate signal of present stage.

PPA viz. Kogge-Stone Adder (KSA) uses a binary tree structure to generate the carry signals in parallel and is known for its low delay[8],Brent-Kung Adder(BKA) with binary tree structure, but with fewer levels than the Kogge-Stone Adder with low complexity and low delay[9], Han-Carlson Adder (HCA)using a tree structure with four input bits per node to generate the carry signals in parallel ensuring low power consumption[10] and Ladner-Fischer Adder (LFA) using a tree structure with two input bits per node to generate the carry signals in parallel known for its simplicity and low hardware cost[11].

In this paper, four filter banks are designed using the above four PPA adders, and the filterbank performance is compared in terms of power and resource utilization. The filterbanks are designed using Verilog HDL on Vivado 2018, synthesized on Xilinx XST, and simulated on ISim simulator of the Xilinx Vivado tool.

The key contributions of this paper are:
1. Analysis of important parametric performance parameters in view of hearing aid application and role of adders and filterbank in their design.
2. Design of FRM based filter model on MATLAB and obtaining the best coefficients.
3. Design, simulation and synthesis of four types of parallel prefix adder and their comparative evaluation based on resource utilization
4. Design, simulation and synthesis of filterbank with four types of PPA and their performance evaluation in terms of power requirement

The structure of the paper is as follows: Section 2 familiarizes with the works related to study. Section 3 discusses proposed methodology for the work under consideration. Section 4 delves into the design of PPA adder-based Filterbanks. Section 5 is devoted to the findings of the comparative study of developed filterbanks employing various PPA-based adders, as well as related discussion. Section 6 summarises the result of this work.

2. Related Work

Hearing aids (HA) which help the masses with hearing disturbance must be personalized to to fit the unique demands of various patients. The key component of digital HA is filter-bank. Choosing the right type of filter bank is crucial to optimizing effectiveness of HA. Uniform filter-bank fails to accommodate individual auditory qualities and auditory properties of distinct hearing loss patients leading to insufficient audiogram fitting performance [12]. As a result, researchers have paid close attention to the non-uniform filters and are regarded as a apt option for HA[13]. Several studies had been done on the filter-bank design for hearing aid application over the past decades. An elaborative review of various filter-bank design approaches for hearing aid is given in[14]. In [15, 16], authors have presented a bird's-eye perspective of cutting-edge ways for designing Reconfigurable filters. As low computational and hardware complexity is required for hearing aid design, many researchers have made a move in the direction of Distributed arithmetic technique for filter design where conventional multipliers are replaced by adders, lookup tables and shift registers [17, 18]. In [19], the author has proposed a multiplierless as well as LUT-less DA architecture for reconfigurable hearing aid. For hearing aid applications, yet another critical requirement is the very sharp narrowband filters with low transitional bandwidth and a large number of sparse coefficients. The FRM method allows for such a design thus requiring lesser hardware architecture and reduced computational complexity [20-24]. To add reconfigurability to the system so as to achieve better audiogram matching and improved auditory compensation for hearing impaired, authors proposed reconfigurable filter in form of variable bandwidth filters using digital spectral transformation[25], using farrow structure[26], using fractional fourier transform[27] and using frequency warping technique[28]. An extensive literature review indicates that there is still a pressing demand for improved reconfigurability in filterbanks with optimum power requirements and reduced hardware requirements and complexity. The proposed research work is inspired by this research need and intends to design low-power reconfigurable filter bank using adders with minimum resource utilization.

3. Proposed Method

The proposed research design work comprises of FRM filter Model designed on MATLAB and the Filterbank with its processing Unit designed using Verilog HDL on Xilinx vivado and implemented on FPGA 7 series Genesys 2 target device. The inputs to the design are the digital audio samples and the pre-computed filter coefficients generated from the FRM filter model. The output of the system is an analog processed output signal generated obtained through

the audio codec of the Genesys 2 FPGA board as shown in Figure 4.

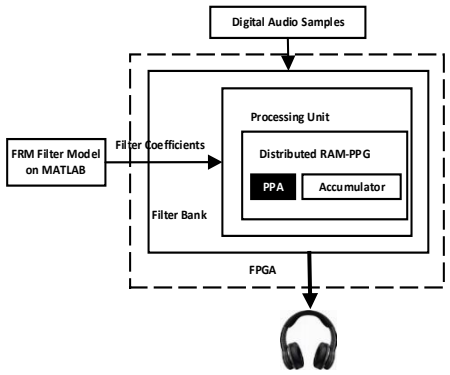

Fig 4. Proposed research design

The complete flow of the research work is divided into following stages as shown in Figure 5.

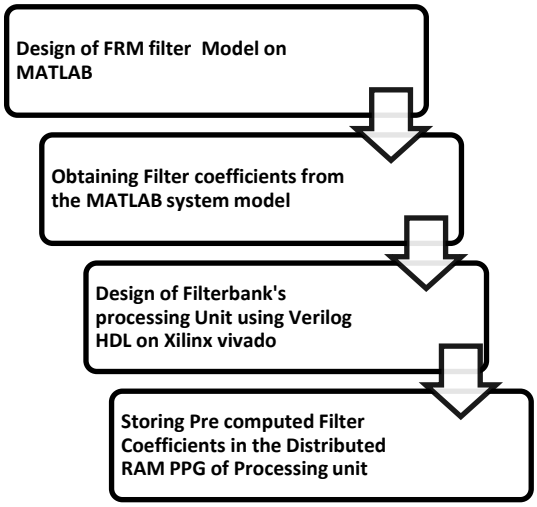

Fig 5. Flowchart of proposed design method

Stage I: Design of FRM filter Model on MATLAB

The system model of the Filter is designed in MATLAB using FRM method as shown in Figure 6. The FRM-based filter is chosen as it reduces computational complexity and improves frequency shaping and compensation in hearing aids.

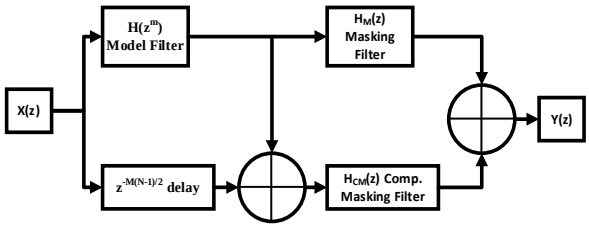

Fig 6. System model of the FRM Filter

The proposed FRM model transfer function Y(z) is given as shown in equation (9).

$$Y(z) = H(zM)\,HM(z) + HC(zM)\,HCM(z) \quad (9)$$

Where H(z) represents a low pass linear phase model filter and its complementary model filter $H_c(z)$ as $H_c(z) = z^{-M(N-1)/2} - H(z)$. Interpolating both H(z) and $H_c(z)$ by factor M, periodic model filter $H(z^M)$ and complementary periodic model filter $H_C(z^M)$ are obtained. These two filters' transition width is significantly reduced by 1/M times the original. The filters $H(z^M)$ and $H_C(z^M)$ are cascaded to the masking filters $H_M(z)$ and $H_{CM}(z)$ respectively, which suppress the unwanted portions of $H(z^M)$ and $H_C(z^M)$.

Stage II: Obtaining Filter coefficients from the MATLAB system model

Based on the design parameters set for hearing aid application, the following set of filter coefficients have been obtained from the MATLAB filter model as depicted in Table 1.

Table 1. Filter coefficients obtained from proposed FRM filter designed on MATLAB

Coefficient	Values
h(0) = h(44)	0.000219970958237
h(1) = h(43)	0.000114454809802
h(2) = h(42)	-0.000802764151062
h(3) = h(41)	-0.002561006035400
h(4) = h(40)	-0.003855280510825
h(5) = h(39)	-0.002617559966678
h(6) = h(38)	0.001825152451519
h(7) = h(37)	0.006756221902118
h(8) = h(36)	0.007035185245136
h(9) = h(35)	-0.000271153016967
h(10) = h(34)	-0.011139963144638
h(11) = h(33)	-0.015391302383321
h(12) = h(32)	-0.005003970063579
h(13) = h(31)	0.015866668224653
h(14) = h(30)	0.029561623256230
h(15) = h(29)	0.017590270813397
h(16) = h(28)	-0.020132227522036
h(17) = h(27)	-0.056343428240625
h(18) = h(26)	-0.050023401316209
h(19) = h(25)	0.023107308494801
h(20) = h(24)	0.145681212438898
h(21) = h(23)	0.261622593435563
h(22)	0.309160333127354

Stage III: Design of Filter's Processing Unit using Verilog HDL on Xilinx Vivado

The processing unit of the proposed filter design comprises of a set of DRAM partial product generators (PPG) and a Parallel Prefix adder structure for summation. The outputs of PPA are accumulated by shift-accumulator. It is followed by the shift accumulator for the shifting of partial products.

Stage IV: Storing Pre-computed Filter Coefficients in the Distributed RAM structure of Processing Unit

These pre-computed filter coefficients are then stored in the Distributed RAM structure of Processing Unit (PU) of the Filterbank designed using Verilog HDL on Xilinx Vivado 2018.

For hearing aid applications, power consumption is a critical design consideration due to the limited battery life and small form factor of the device. Use of an appropriate type of adder in the filter bank of hearing aid can play a crucial role in reducing power consumption and design complexity. With this aim in mind, four types of Parallel prefix adders have been used in the designed filterbank structure and their performance has been compared in terms of power consumption. The flow of this design and comparative analysis is presented in Figure 7.

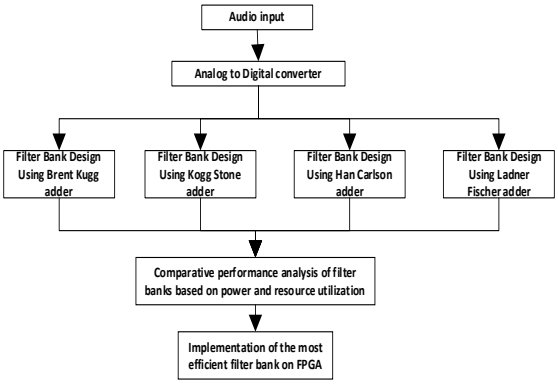

Fig 7. Complete overview of proposed Research work

4. Results and Discussion

The section presents the obtained experimental results in form of synthesis results of the four different filter banks designed using four different parallel prefix adders as modules viz. BKA, KSA, HCA and LFA in Verilog HDL on Xilinx Vivado 2018 tool. The results further confirm the functional correctness of the design by validating their testbench simulation results.

In the discussion part of the section, the comparative analysis of the four adders is performed in terms of their resource utilization to check their aptness for use in the filterbank of hearing aid. The impact of all four PPA as adder modules on the filterbank design performance was further analyzed by comparing the filterbanks in terms of their power utilization and the optimum filterbank with the lowest power consumption is highlighted at the end of this section.

4.1. Synthesis and Simulation results of 8-bit Parallel Prefix Adders and their parametric comparison

This subsection presents the Synthesis and Simulation results of 8-bit PPAs. The RTL schematic and testbench simulation results of 8 bit BKA designed in Vivado 2018 is depicted in Figure 8 and Figure 9.

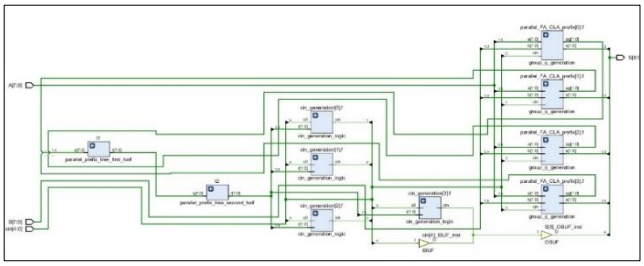

Fig 8. RTL schematics of BKA

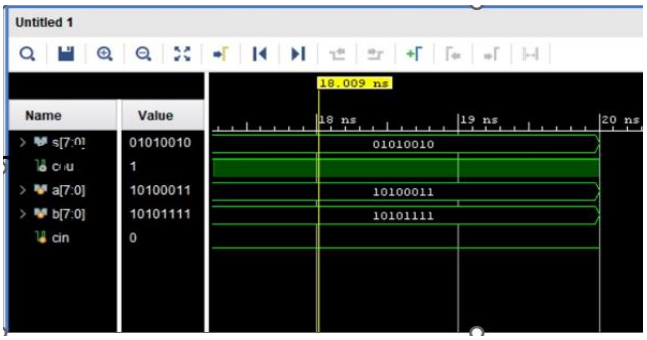

Fig 9. Simulation result of 8-bit BKA

The RTL schematic and testbench simulation results of 8 bit KSA designed in vivado 2018 is shown in Figure 10 and Figure 11.

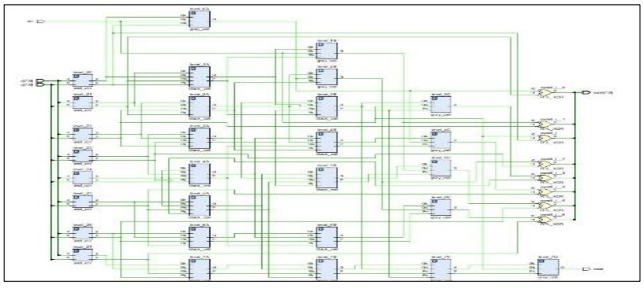

Fig 10. RTL schematics of KSA

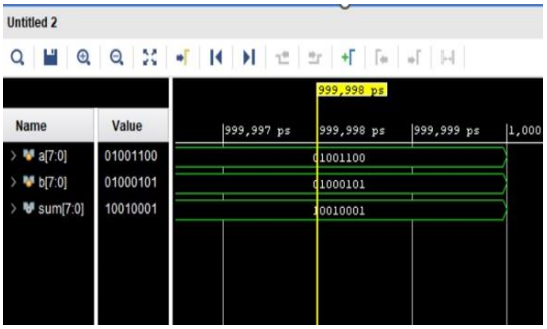

Fig 11. Simulation result of 8-bit KSA

The RTL schematic and testbench simulation results of 8 bit HCA designed in vivado 2018 is depicted in Figure 12. and Figure 13.

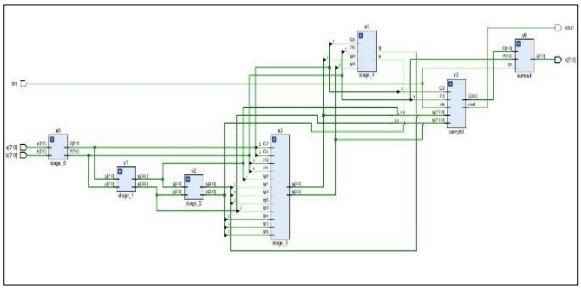

Fig 12. RTL schematics of HCA

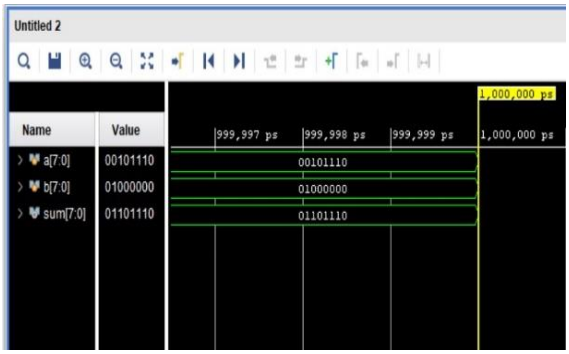

Fig 13. Simulation result of 8-bit HCA

The RTL schematic and testbench simulation results of 8 bit KSA designed in vivado 2018 is presented in Figure 14 and Figure 15.

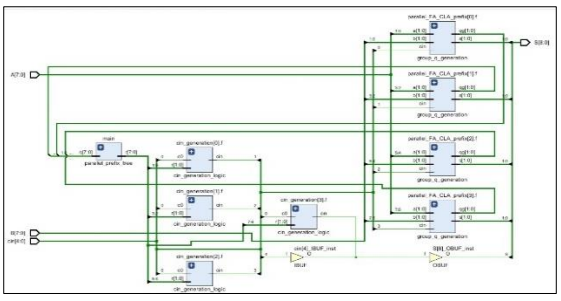

Fig 14. RTL schematics of LFA

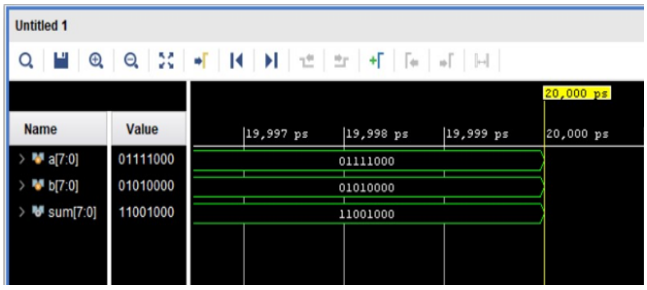

Fig 15. Simulation result of 8-bit LFA

For hearing aid applications, hardware complexity and area requirement are crucial concerns. The resources utilized by adders used in filterbank will in turn significantly impact the hardware complexity and requirement of the HA. With this aim in mind, the synthesis reports of all four 8-bit adders are analyzed and compared in terms of their resource utilization which is reported in Table 2.

Table 2. Comparative analysis of adder's resource utilizations

Parameter	BKA	KSA	HCA	LFA	Available
Slice	3	5	5	3	50950
Slice LUTs	8	14	11	7	203800
Number of bounded IOBs	26	24	24	24	500
% Utilization of IOBs	5.20	4.80	4.80	4.80	100

4.2. Synthesis and Simulation results of Filter banks and their parametric comparison

For hearing aids, filter bank is then designed taking into consideration the design requirements and constraints of the application at hand. Each filter of the filter bank comprises the Processing Units as the main internal design block. The RTL schematic of the filter bank designed in Xilinx Vivado and synthesized using XST tool is shown in Figure 16.

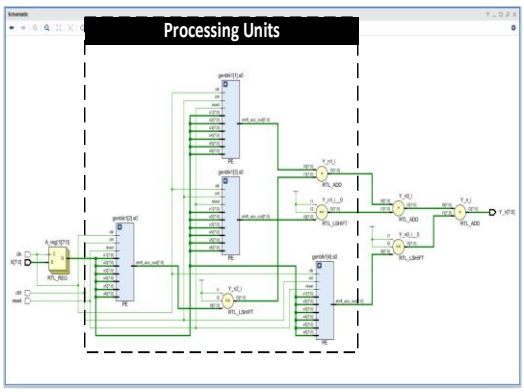

Fig 16. Complete RTL Schematic of proposed Filter structure

highlighting PU block

The adders designed in Verilog HDL presented in the previous subsection are then used as components in the processing unit of the proposed filterbank. In this PPA-based filterbank, the PU section majorly comprises Distributed RAM PPG and Brent Kung adder as the internal components of the schematic as shown in Figure 17.

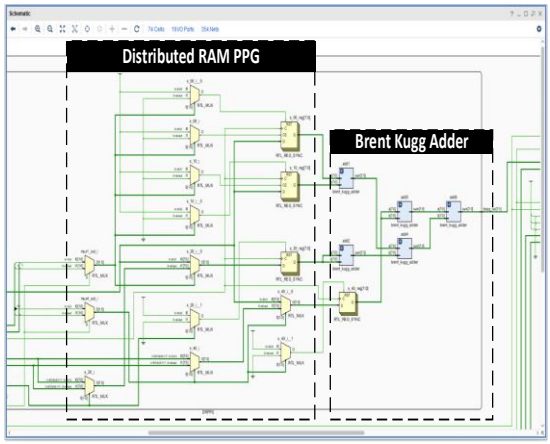

Fig 17. RTL Schematic of PU block with DRPPG and BK Adder modules

The filter designed using KS adder as the internal component is synthesized using XST tool of Xilinx Vivado 2018 as shown in Figure 18.

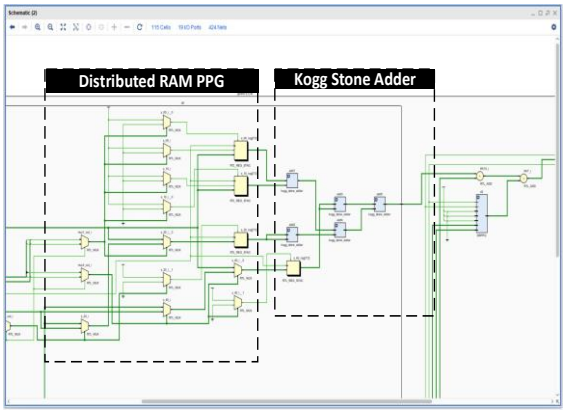

Fig 18. RTL Schematic of PU block with DRPPG and KS Adder modules

The filter variant designed using HCA is then synthesized and its RTL schematic is shown in Figure 19.

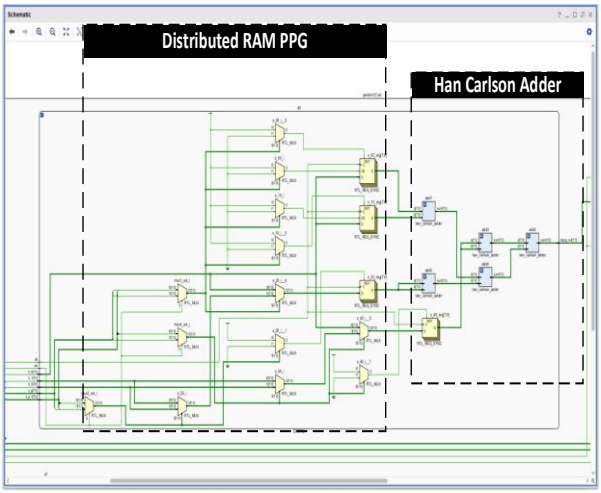

Fig 19. RTL Schematic of PU block with DRPPG and HC Adder modules

The fourth variant of the proposed filter is then designed using LF adder and its RTL schematic is depicted in Figure 20.

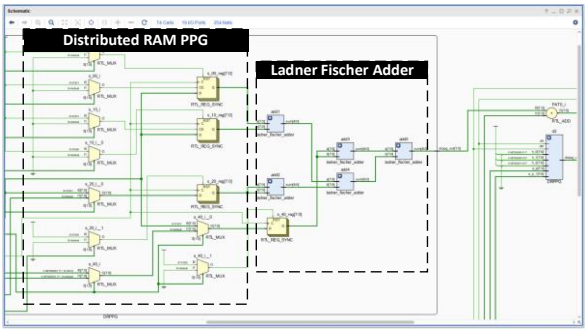

Fig 20. RTL Schematic of PU block with DRPPG and LF Adder modules

These four variants of proposed filter structure using four different types of PPA are later checked for their functional correctness by writing their testbench and are simulated using the Isim of Xilinx Vivado tool. The simulation results of all four filter structures designed using BKA, KSA, HCA and LFA is presented in Figure 21, Figure 22, Figure 23 and Figure 24 respectively.

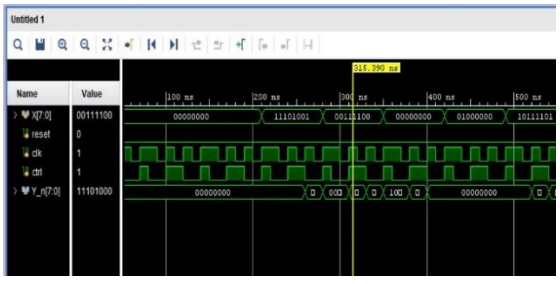

Fig 21. Simulation result of Filter with BK Adder

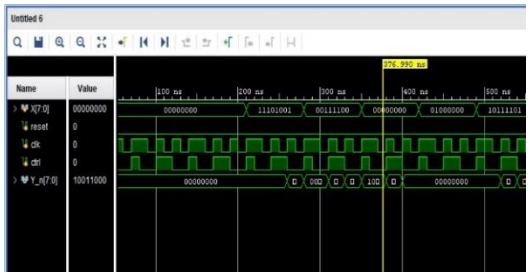

Fig 22. Simulation result of Filter with KS Adder

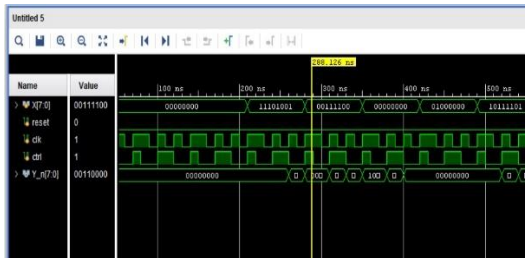

Fig 23. Simulation result of Filter with HC Adder

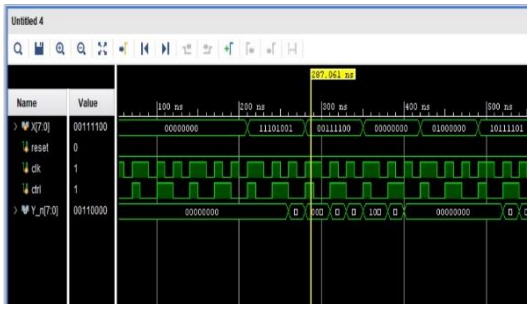

Fig 24. Simulation result of Filter with LF Adder

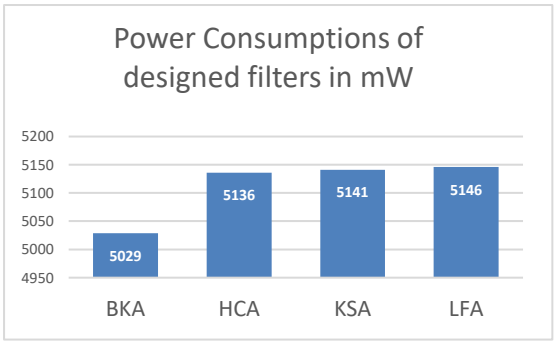

Fig 25: Comparative power analysis of Filters using various PPA

Table 3. Comparative analysis of resource utilization of filterbanks.

Resource Utilization	Filter with BKA	Filter with KSA	Filter with HCA	Filter with LFA	Available Resources
Slice	12	10	10	10	50950
Slice LUTs	18	18	18	18	203800
Number of bounded IOBs	14	14	14	14	500
% Utilization of IOBs	5.20	4.80	4.80	4.80	100
Slice Register	16	16	16	16	407600
LUT as Logic	18	18	18	18	203800
LUT Flip-Flop Pairs	8	8	8	8	203800

Table 4. Power comparison of Proposed vs. Existing reconfigurable Filter

Filter design	Power Consumption (in mW)	% improvement w.r.t existing design[29]
Reconfigurable Filter using BKA*	5029	39.74
Reconfigurable Filter using KSA*	5136	38.45
Reconfigurable Filter using HCA*	5141	38.39
Reconfigurable Filter using LFA*	5146	38.33
Reconfigurable Filter using Carry Bypass Adder# [29]	8345	

* Proposed Designs
\# Existing design

4.3. Discussion on the results

The results obtained from our experimental study reinforce the potential of Parallel Prefix Adders (PPAs) as a key component in power-efficient, reconfigurable Frequency Response Masking (FRM) filter banks for hearing aids. The main highlight from the experimental results is the excellent performance of the Brent Kung Adder (BKA)-based reconfigurable filter bank, which surpassed other designs in power efficiency as depicted in Table 4.

PPAs such as the Kogge-Stone Adder (KSA), Han-Carlson Adder (HCA), and Ladner-Fischer Adder (LFA), while providing efficient operation, were outperformed by the BKA in the context of our design. The BKA-based reconfigurable filter bank recorded the least power requirement, consuming 39.74% less power compared to the existing reconfigurable filter design that used a Carry Bypass adder. This validates our hypothesis that the choice of adder can significantly impact the power utilization of reconfigurable FRM filter-banks in hearing aids.

The application of Distributed Arithmetic technique to generate distributed RAM partial product generators further contributed to power efficiency.

However, the gains realized through this technique were significantly amplified by the incorporation of the BKA, indicating a synergistic effect between the design techniques used. The performance of the BKA in this study aligns with previous research that highlighted its lower power consumption and high-speed performance. This research, therefore, confirms the suitability of BKA for power-critical applications such as hearing aids.

The application of the BKA also supports the pursuit of customized and flexible hearing aid designs. Given the lower power requirements of BKA-based filter banks, there is potential for hearing aids with longer battery life, potentially lighter weight, and enhanced user comfort. However, it should be noted that this research, while promising, is based on simulated implementations. Further research will be necessary to confirm these findings in real-world applications. We also recognize that there may be other factors, such as the cost of components and complexity of integration, that could impact the feasibility of applying our design in commercial hearing aids. These factors would benefit from further study and analysis.

5. Conclusion

In this research, we proposed a new and more power-efficient design for a reconfigurable Frequency Response Masking (FRM) filter bank using a Brent Kung Adder, specifically intended for use in hearing aid devices. Main objective of research was to improve power efficiency and performance without compromising the audio quality and response of the hearing aids. The Brent Kung adder was chosen for its low power consumption and high-speed performance with reduced resource utilization, outperforming traditional binary adders. When integrated into the FRM filter bank, it resulted in a significant reduction in power usage of the filter operation. Simulations were conducted to assess efficiency of proposed design, and the results were satisfactory. The reconfigurable FRM filter bank showcased a noteworthy improvement of 39.74% in power efficiency over the existing Reconfigurable filter using carry Bypass adder without sacrificing the quality of sound reproduction, thus making it a viable solution for hearing aids, where power efficiency and audio quality are critical parameters. Despite the encouraging results, further improvements can be made. Future work will delve into optimizing the power usage and speed further, as well as researching ways to miniaturize the design to ensure it fits comfortably in a wide range of hearing aid designs. In conclusion, our research has demonstrated the potential benefits of integrating a Brent Kung adder in an FRM filter bank for hearing aids. This could potentially lead to the development of more efficient, customized, and user-friendly hearing aids in the future.

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Conflicts of interest

The authors declare no conflicts of interest.

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