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Optimizing Digital PWM Techniques for DC-DC Converters in Software-Defined Radios (SDRs): A Robust Architectural Approach

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Abstract*:* The rising demand for Software-Defined Radios (SDRs) necessitates innovative solutions for efficient power management. This paper explores the use of an FPGA-based Digital Pulse Width Modulation (DPWM) technique to enhance the performance of DC-DC converters in SDRs. The primary objective is to develop and assess the effectiveness of this FPGA-based DPWM approach in improving power conversion efficiency, adaptability, and overall SDR performance. Our method involves creating and implementing an FPGA-based PWM control strategy, synthesizing the DPWM architecture through Verilog and Xilinx ISE Design Suite 14.1. Subsequently, we integrate this PWM technique into SDR DC-DC converters and conduct a thorough evaluation using MATLAB Simulink and a digital storage oscilloscope. The DPWM architecture achieved an impressive 189.17 MHz operating frequency, resulting in significant enhancements in power conversion efficiency, dynamic power demand responsiveness, and notable reductions in power losses. In conclusion, the integration of FPGA-based PWM in SDR DC-DC converters represents a promising solution to enhance power management. It holds the potential to advance SDR technology by increasing efficiency and adaptability to address the evolving demands of wireless communication systems.

Keyword*- Digital Pulse Width Modulator, DC-DC converter, FPGA, Software-Defined Radios.*

1. Introduction

DC to DC converters are essential components in many communication devices and power electronic systems, including renewable energy systems, Software Defined Radios [SDR], battery charging systems, and electric vehicles [1]. These converters regulate the output voltage and current by adjusting the duty cycle of the switching signals that drive the power MOSFETs. Digital Pulse Width Modulation controllers generate these switching signals based on a reference signal and a feedback signal. In recent years, Field Programmable Gate Arrays (FPGAs) have become popular for implementing digital pulse width modulation (DPWM) controllers due to their high flexibility, low latency capabilities and ability to implement complex control algorithms.

FPGA-based DPWM controllers offer high flexibility because they are reprogrammable to implement different control algorithms and modulation schemes. Analog based design are fixed in their configuration and control strategy. In FPGA-based controllers, designers can adjust the control strategy to meet the specific requirements of their DC to DC converter without modifying the hardware. This feature can reduce the time and cost of development and make it easier to implement different control algorithms and modulation schemes.

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FPGA-based DPWM controllers offer low latency. Unlike traditional analog controllers, which require control signals to e processed through several analog components, FPGA-based controllers generate the switching signals directly from digital signals. This eliminates the delay caused by the analog processing, resulting in faster response. Faster response times are important for high-performance in software defined radios. Especially those that require fast transient response or high switching frequencies.

FPGA-based DPWM controllers have ability to implement advanced control algorithms. For example, digital current sensing can be implemented in the FPGA, providing more precise and authentic current measurements compared to traditional analog methods. It gives more control over the output voltage and reduces the overloading risk in the system. Additionally, adaptive voltage control and feed forward compensation can be implemented in the FPGA to improve the stability of the system under changing load conditions.[25]

FPGA-based DPWM controllers can also enable implementation of advanced digital signal processing techniques. For example, frequency domain analysis can be used to analyse the system's behaviour in the frequency domain and identify potential sources of unreliability or inefficiency. This information can be used to adjust the control algorithm and modulation scheme to further improve the performance of the DC to DC converters in SDR.

FPGA-based DPWM controllers offer many advantages over traditional analog controllers for DC to DC converters. They offer high pliability, low latency, and the ability to implement advanced control algorithms and digital signal processing techniques. These features can help designers to develop high-performance SDR's and electronic systems with improved efficiency, reliability, and stability.

2. Literature Survey

The industry of FPGA grew by PLDS (Programmable logic devices) and PROM (Programmable read-only memory). Both PLD and PROM were having an alternative of getting programmed in an industrial facility/field (field programmable) in groups. In case, between the logic gates, the programmable logic has been hard wired.

This work focuses on examining the DC-DC buck converter's performance in the context of renewable energy applications. Renewable energy sources typically generate direct current (DC) voltages, necessitating the use of DC-DC converters to adapt these voltages for various applications. n this study[2], a DC-DC buck converter is employed to reduce high-level DC voltage to a lower level. The converter's output voltage characteristics are investigated by altering the duty cycle. Simulations are carried out using PSIM and verified through practical hardware implementation.

This paper will investigate and contrast the simulation, comparison, and implementation of multiple controllers integrated into a single chip with the use of distinct individual controllers on a chip in the context of a DC-DC converter [3] and its associated application. Specifically, the study employs a PID controller for the DC-DC converter and a PI controller for the actuator, with the analysis conducted using MATLAB/Simulink, Xilinx, and Modelsim. These methodologies were tested on a Spartan-3E FPGA for evaluation and experimentation.[3], there are three main blocks used in this design.1-DC-DC Converter,2-Actuator and 3-Field Programmable gate array. DC-DC Converter block has the circuit of boost converter. It uses to amplify or boost the fixed input level signal to actuator required variable level. The circuit has 3 main components Inductor Capacitor, diode and switch(MOSFET).This MOSFET switch is digital controlled by the PWM generator circuit blocks.

This study presents a DC-DC buck converter featuring a pulse width modulation (PWM) feedback control system, accommodating a power supply voltage range from VDD to 2.5 times VDD, equivalent to 5-14 volts[4]. This converter is a compact single chip, occupying an area of 1.379 by 0.813 square mili meters and is fabricated using a 0.5-micron HV CMOS process. The chip incorporates high-voltage (HV) MOSFETs, a Dead-time detector, a PWM feedback loop, a control circuit, and HV driving transistors. The primary innovation of this design lies in its ability to deactivate an optimal number of power MOSFETs during light load conditions, resulting in remarkably high conversion efficiency. Importantly, the effectiveness of this solution is analytically validated, achieving a light load efficiency increase from 31.71%, as typically achieved through traditional methods, to an impressive 67.94% through the proposed design.

This study focuses on addressing the power supply requirements for aircraft equipment, specifically in the context of high voltage DC-DC power converters. The research begins by exploring the topological structure of the High Voltage DC-DC Converter (HVDC) and proceeds to outline the design of the starting circuit, which is based on the TL3844 control chip. Additionally, it introduces a method for calculating component parameters[5]. The paper suggests a straightforward approach to enhance power output. It also includes the design of a protection circuit that incorporates over-current protection (OCP) and over-voltage protection (OVP) to enhance the stability of the supply system. Furthermore, a voltage compensation circuit is designed to address voltage discrepancies. The study concludes by confirming the viability of the module through experimental validation during real converter operation.

This paper introduces an improved method for enhancing the performance of a linear buck converter system employed in mobile devices, specifically smartphones. This enhancement is achieved through the utilization of an adaptive digital Proportional-Integral-Derivative (PID) controller in conjunction with an offline swarm optimization algorithm. The primary objective of this research is to enhance the control of the linear buck converter system using a single-input single-output (SISO) digital Field Programmable Gate Array (FPGA)-PID controller[6]. The adaptive SISO-FPGA-PID voltage-tracking controller proposed in this study aims to swiftly and accurately determine the optimal voltage control action, represented by the optimal on-off duration time. This control action is crucial for regulating the output voltage of the buck converter and preventing hardware issues in mobile devices. To achieve this optimization, the Particle Swarm Optimization (PSO) algorithm is employed to identify and fine-tune the three key parameters of the SISO-FPGA-PID controller.

3. Design and Parameters.

Digital Clock Modulator:

Digital Clock Modulators (DCMs), are specialized digital circuits used in high-performance, high-frequency applications to handle clock signals. By directly incorporating sophisticated clocking capabilities into the

global clock distribution network, they are intended to address common clocking challenges including clock skew and distribution delays.

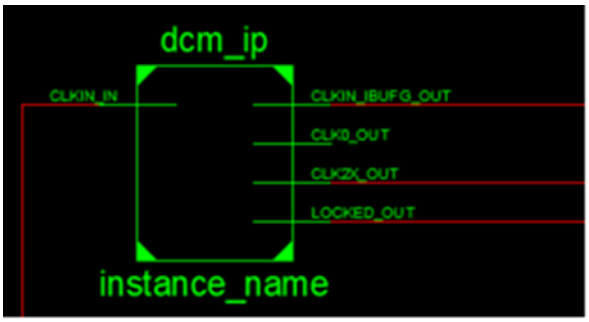

Fig 1.RTL schematic of Digital clock Modulator.

Fig1 shows the schematic diagram of digital clock modulator. Clock skew or the discrepancy in a clock signal's arrival times at various places in the system, is one of the key advantages of DCMs. By ensuring that all clock signals reach their intended locations simultaneously. This can considerably enhance system performance as a whole. Phase shifting, frequency synthesis, clock conditioning, and clock signal conversion are among the additional features that DCMs offer. For instance, DCMs can double or divide an input clock frequency or synthesise an entirely new frequency. They can also phase shift a clock signal by a fixed fraction of a clock period or by incremental amounts. Additionally, by conditioning a clock with DCMs, a clean output clock with a 50% duty cycle is guaranteed. They can also check clock skew and convert an incoming clock signal to a different I/O standard by mirroring, forwarding, or rebuffering the clock signal. Spread-spectrum clock generation, a free-running oscillator, and clock input jitter filtering are further aspects of DCMs. In high-performance, high-frequency applications, these properties contribute to an improvement in the performance and dependability of clock signals.

Freq_out_clock = Fin_in_clock * scaling_factor * Freq_val.. (1)

The frequency of an output clock signal is determined using the formula given in equation-(1) This is the desired frequency of the output clock signal, or Freq_out_clock.

Fin_in_clock: The frequency of the input clock signal that you are utilizing as a guide to produce the output clock signal is indicated here.

Scaling_factor: This quantity is used to adjust the frequency of the input clock in order to produce the desired output clock frequency. Although it can be any integer value, it is frequently a power of two. As a multiple or fraction of the input clock frequency, the variable as a multiple or fraction of the input clock frequency.

Freq_val: This is a value that's used to specify the desired output clock frequency as a fraction or multiple of the input clock frequency.

According to the equation-1, we can multiply the frequency of the input clock signal (Fin_in_clock) by a scaling factor and a frequency value (Freq_val) that specifies the desired output frequency as a ratio or multiple of the input frequency in order to produce an output clock signal with frequency F_out_clock.

Here is an illustration of how you could apply to F_out_clock.:

Assume that you wish to produce an output clock signal with a frequency of 50 MHz from a 100 MHz input clock signal. The following formula, using a scaling factor of 1 and a frequency value of 0.5

F_out_clock = 50 MHz = 100 MHz * 1 * 0.5

The output clock signal would have a frequency of 50 MHz, which is half that of the input clock signal, as a result.

Table-1 characteristics of a Digital Clock Manager (DCM) and the corresponding DCM signals.

Feature	Description	DCM Signals
DCMs per device	Four to 12 DCMs, depending on device size.	All
Clock input sources	GCLK input, BUFG output, cascaded DCM or PLL output (within the same CMT). General interconnect is allowed but not recommended for optimal performance	CLKIN
Frequency synthesizer output	Multiply CLKIN by the fraction (M/D) where M = {2..256}, D = {1..256} when using the DCM_CLKGEN primitive	CLKFX, CLKFX180
Clock divider output	Divide CLKIN by 1.5, 2, 2.5, 3, 3.5, 4, 4.5, 5, 5.5, 6, 6.5, 7, 7.5, 8, 9, 10, 11, 12, 13, 14, 15, or 16	CLKDV
Clock doubler output	Multiply CLKIN frequency by 2	CLK2X, CLK2X180
Clock conditioning,	Always provided on most outputs	All

duty-cycle correction		
Quadrant phase-shift outputs	0° (no phase shift), 90° (¼ period), 180° (½ period), 270° (¾ period)	CLK0, CLK90, CLK180, CLK270
Half-period phase-shift	Output pairs with 0º and 180º phase shift, ideal for	CLK0, CLK180,
outputs	DDR applications	CLK2X, CLK2X180, CLKFX, CLKFX180
General purpose DCM operation indicators	Number of DCM clock outputs connected to general purpose inter connect	STATUS, LOCKED

Depending on the size of the device, there can be four to twelve DCMs available. Clock input sources: DCMs can accept clock inputs from various sources, including GCLK input, BUFG output, cascaded DCM, or PLL output within the same CMT (Clock Management Tile). While it's possible to use general interconnect for these sources, it's not recommended for optimal performance. The primary clock input is referred to as CLKIN. In summary, the table-1 provides a detailed overview of the features and DCM signals associated with clock management in a device

Grey Counter:

In digital pulse width modulation (PWM) using a DC-DC converter, a grey counter is a binary counter that counts in a specific sequence of binary numbers, producing a waveform with a grey code. This technique allows for precise control of the duty cycle, and thus the output voltage of the converter, which is essential in applications such as power supplies, motor control, and LED lighting.

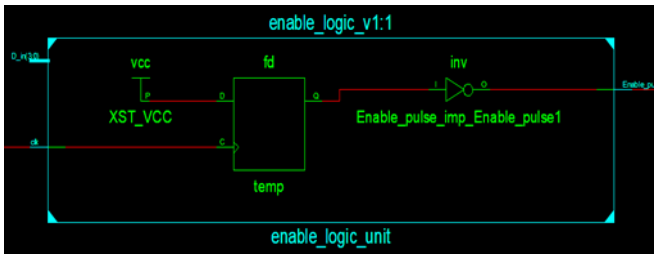

Fig 2.RTL Schematic of Grey counter

The grey code produced by the counter ensures that there are no glitches or sudden changes in the output waveform when the counter value changes. This property of the grey code makes it valuable in achieving stable and efficient output voltage regulation in power supplies, the grey counter is a key component in digital PWM control of DC-DC converters used in SDR. Its ability to produce a waveform with a grey code and enable precise control of the duty cycle allows for precise control of the output voltage, making it a valuable technique in various applications.

One Hot Encoder:

In digital pulse width modulation (PWM) systems, a one hot encoder is a type of binary counter that counts through a sequence of binary numbers using a one hot code.

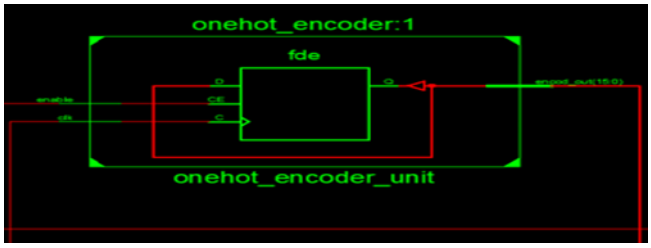

Fig 3.RTL schematic of Onehot encoder.

The one hot code is a binary code in which only one bit is set to 1 at any given time. This allows for clear identification of each binary value, enabling efficient and accurate encoding of digital signals. By using a one hot encoder to generate a PWM signal, it is possible to achieve precise control over the output waveform, making it a valuable technique in various applications such as Power converter of DC-DC signals, motor control, LED lighting.

Pulse Width modulation controller:

In the Digital Pulse Width Modulation (DPWM) technique project that uses a DC-DC converter, PWM plays a crucial role in regulating the power delivered to the SDR internal devices and Loads. Fig 4 shows the RTL schematic of the PWM controller.[26]

The PWM signal is generated based on input signals from the DCM detector, grey counter, one hot encoder, and feedback loop, and is used to control the switching of power MOSFETs or transistors in the converter. This allows for precise control of the output voltage or current, enabling stable and efficient operation of the converter. Overall, PWM is essential in ensuring reliable and consistent power delivery to the SDR module in the DPWM technique.

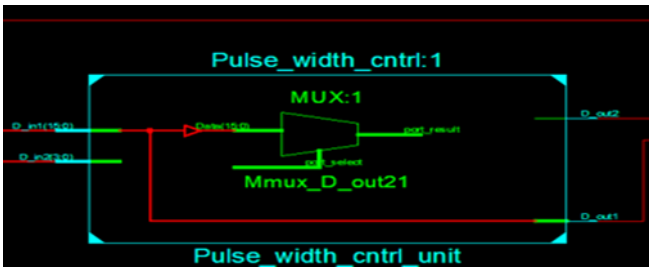

Fig.4 : RTL schematic of the PWM controller.

Duty Cycle:

Digital Pulse Width Modulation (DPWM) technique using in a DC-DC converter, the duty cycle is the ratio of the pulse width to the period of the PWM signal it is shown in equation-2. It represents the percentage of time that the pulse is "on" or high, compared to the total time of the signal. The duty cycle is an important parameter in the DPWM technique project, as it determines the average voltage or current delivered to the load. By adjusting the duty cycle, the power delivered to the load can be regulated, allowing for stable and efficient operation of the converter. The duty cycle is typically controlled by the one-hot encoder block, which receives input signals from the feedback loop and generates a binary code that determines the duty cycle of the PWM signal. By changing the binary code, the duty cycle can be adjusted to maintain output voltage regulation.

$$D = Ton / T \qquad (2)$$

The duty cycle of a periodic waveform is calculated using the formula. Below is each of the formula variables stands for:

D: This represents the waveform's duty cycle, which is given as a percentage or decimal fraction between 0 and 1.

Ton: This is the length of the waveform's "on" or "high", which is typically expressed in seconds.

T: This is the waveform's period, which is the length of a single full cycle and is often expressed in seconds.

By dividing the length of the "on" part (Ton ne) by the waveform's period (T) and multiplying the result by 100 if you wish to represent the duty cycle as percentage as shown in equation-3, you may determine the waveform's duty cycle using this formula.

$$D = (Ton / T) * 100\% \qquad (3).$$

As an alternative, you can eliminate the 100% multiplication and instead specify the duty cycle as a decimal fraction between 0 and 1. Here, the equation is as same as equation 2.

Consider a periodic waveform with a period of 10 milliseconds (0.01 seconds) and a "on" period of 3 milliseconds (0.003 seconds), for instance. You can use the equation-2 and 3 to get the waveform's duty cycle:

D = (0.003 s / 0.01 s) * 100% = 30%

This indicates that the waveform is "off" or "low" for the remaining 70% of the time, and "on" or "high" for the remaining 30%.

Implementation of Boost and Buck Converter using FPGA and MAT Lab Simulink tool

Switching mode sources can be used for a variety of tasks as well as for a DC chopper. Although DC supplies, such as batteries, are rechargeable, Whether or not a battery bank is used, additional mass and building space requirements will be substantially larger.

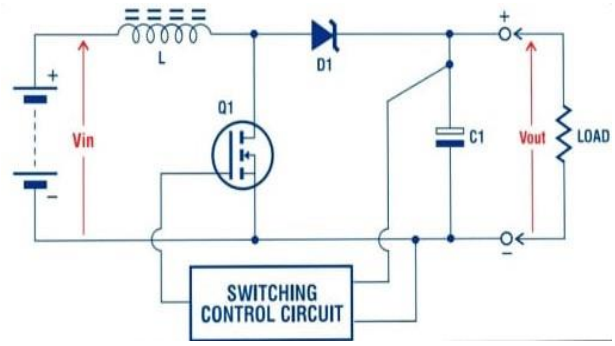

Fig 5: Boost converter design using Simulink tool

The solution to the problem is to use less batteries, which forces you to boost the voltage (DC) to the necessary point. Another problem with batteries is that, whether they are tiny or large, the incoming voltage changes as available energy is used. Eventually, the battery voltage becomes too low to be considered for powering the specified circuit. Utilising a boost converter, the battery life is extended as the low output point is raised behind the functional point. In starting there is a lot of circuit activity when a square wave with a high frequency is applied to the MOSFET gate terminal. When a short circuit is created, the MOSFET conducts for the period of L1, supplying the input's negative terminal. Therefore, the charge moves between negative and positive terminals via L1 for supply, and this stores energy in the magnetic field. Practically little current flows through the rest of the circuit because the configuration of the capacitor C1, load, and DI indicates a larger impedance than would be the case with a simple MOSFET-based conductor.

When implementing a buck/boost converter, the values of the output capacitor and the inductor are crucial for the converter's performance and stability. The capacitor and inductor values are chosen based on the desired output voltage, load current, switching frequency, and other specifications.

Calculating the Output Capacitor (Cout): The output capacitor is responsible for filtering and stabilizing the output voltage. The capacitance value is typically chosen to meet the following criteria:

a. Ripple Voltage **(ΔVout):** Determine the allowable ripple voltage in buck/boost converter output. Load Current **(Iout):** Know the maximum load current the converter needs to support. Switching Frequency (**fsw):** The operating frequency of the buck converter.

The equation-4 is to illustrate how we are calculating the output capacitor value.

$$Cout \geq Iout / (fsw * \Delta Vout) \quad (4)$$

Calculating the Inductor (L) value in Buck and Boost converter.

The inductor in a buck converter stores energy and helps maintain a steady output current. The inductance value is chosen considering the following factors:

Input Voltage **(Vin):** The input voltage range over which the converter operates. Output Voltage **(Vou**t): The desired output voltage. Load Current **(Iout):** The maximum load current. Switching Frequency **(fsw):** The operating frequency of the converter.Duty Cycle **(D):** The ratio of on-time to the switching period, which is given by D = Vout / Vin.

The equation-5 is to calculate the inductance value:

$$L \geq (Vin - Vout) * (D) / (Iout * fsw) \quad (5)$$

Implementation of Buck Converter using FPGA and MAT Lab Simulink tool

When the output DC voltage must be lower than the input DC, the Buck Converter is used. Any DC source can obtain incoming DC. Useful when switching circuits and output don't require isolation, but input still comes from an AC source that has been rectified.

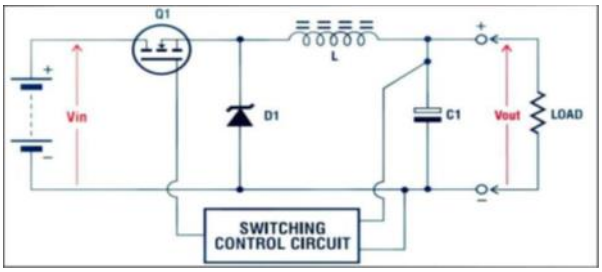

Fig 6: Buck Converter Design in a Simulink tool.

In this scenario, a mains isolating transformer provides isolation between the source and the rectifier. The buck circuit arrangement is shown in Fig6. Flywheel diode DI, switching power MOSFET QI, output filter capacitor CL, and inductor L make up the majority of its parts. A control circuit monitors the voltage leaving the system, maintains Q1 off at the necessary stage and at a controlled pace, but changes D. When QI is turned on, current begins to exit the source through Q1 and L. for C1 and load afterwards. A magnetic field forms at L, causing power to be stored there for a drop across L that lowers some of the incoming voltage. When Q1 is turned off later, L opposes if the current decreases with reverse EMF, and D1 now supplies power to the load. The small quantity of DC output from the input voltage that is visible over L becomes equivalent to D. Consequently,

4. Proposed DPWM Architecture

As per the circumstance the part of unit PWM architecture stand for pulse width Modulator we design the Overview of Entire DPMW Architecture.as shown in the fig (8)

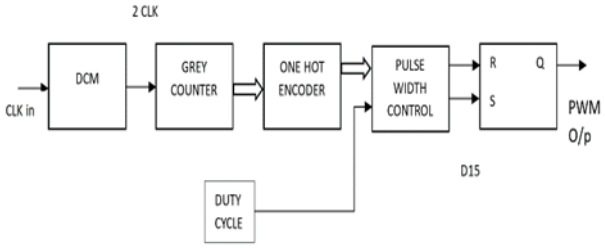

Fig 8: DPWM Architecture.

DCM-The Digital Clock Manager is a component that represent in the electronic Substance there FPGA Spartan 6A can striking with the simulation by the Xilinx. The integrate manipulating the clock signal inside the field programming Gate array. And it can reduce the error in the Circuit therefore the pulse can be controlled by the user and clock force value are handled.

One hot encoder: The one hot encoder required less number of combinational Logic's gates to decode. The each one hot encoder have its own State Variable value. It was Better time margin. It consume the less area and Power Supply

Gray Counter: Grey code is same as the Character of binary code it is also called as reflected binary Code. It is used to check the error and Clarity Correction in binary Communications. It is commonly represented by zeros and ones.

Pulse width control: In this block it will access the feedback from the Outside Circuit, so DPWM pulse are generated automatically by the given voltage.

SR Flip flop: The S R flip flop stands for set and reset the value by leading Edge and ending edge .by this we can see the Exact pulse without any Disturbance.

5. Implementation of Buck Converter using DPWM

Utilizes Digital Clock Manager which Provides control over clock frequency. We can use Multiplies clock input frequency.

4 bit grey counter, 16 bit one hot encoder, RS Flip-flop is used.

Grey counter counts one bit from 0000H to 1000H when the final value is reached, enable signal is generated which is to

set the bit of one hot encoder (From D0-D15 one by one).

When D15 bit (1000 0000 0000 0000) of one hot encoder is one which in turn set the RS Latch which in turn gives PWM output. Then all the bits of One hot encoder resets to zero.

Once again counter starts counting from 0000H to 1000H is reached, enable signal is generated which set the bit of one hot encoder (Till the desired bit is set), which resets the RS flip-flop

PWM output resets after desired bit in one hot encoder set to one depending on duty cycle. The set and reset of RS flip-flop determines the PWM output.

In this article implemented the design on FPGA based digital pulse width modulation controller for dc to dc controller system used in SDR. The output voltage of a dc to dc converter circuit can be Controller by using FPGA board By the Method of (HIL) Hardware in loop Simulation. In this technique we will combine the Hardware and Software together to show the simulation is possible.

In the Matlab we have an inbuilt tool Component called as Digital Controller. This tool will act as a Main Source of PWM and this will be connected to Boost and Buck Controller Separately. So that we can show the waveform and voltage graph separately. In this, Boost Controller will Step up the Voltage and Buck controller step down the voltage(amplitude). In this we can also vary the duty cycle and prove that the voltage can change According to the output value.[15]this shown in equation 6 and equation 7 .

•Boost Controller:

$$Vout = Vin / (I-D) \quad (6)$$

•Buck Controller:

$$Vout = Vin * D \quad (7)$$

• Duty cycle:

Ton /Ton + Toff *100

$$(PWM\_Frequency = 1 / PWM\_Interval\_Period) \quad (8)$$

To determine the proportional PWM output voltage, use this formula: (Duty ÷ 256) x 5 V. For example, if Duty is 100, (100 ÷ 256) x 5 V = 1.953 V;

Pulse width modulation frequency will be calculated by using a equation 8.PWM outputs a train of pulses whose average voltage is 1.953 V. In order to convert PWM into an analog voltage we have to filter out the pulses and store the average voltage[24].

Table 2. Device utilization summary

	Existing Spartan 3A[1]		Available	Proposed Spartan 6	
Logic Utilization	Available	Used	Available	Used	
Number of Slices	704	23	4800	20	
Number of slice flip flops	1408	32	2400	14	
Number of 4 input LUTs	1408	19	25	11	
Number of bonded IOBs	108	8	102	8	
Number of GCLKs	24	2	24	2	
Number of DCMs	2	1	2	1	

In above table-2 illustrate the device utilization summery of digital pulse width modulation architecture, in this architecture compared to earlier work[9] achieved good results in terms of number of flip flop and slice registers and look up table, number of input and output usage, Etc.

Power report of Proposed DPWM.

Table 3. shows the power consumption report of proposed DPWM based DC to DC converter for software defined radio's in this for different clock frequency's we have checked the power consumption report with respect to Sparton 3 and Spartan 6.

Table 3. Power report of proposed work.

Device	Frequency(MHz)	Existing[1]	Proposed
Spartan 3A	6	0.014	----
	12.5	0.0154	----

	15	0.0157	----
	25	0.1573	----
Spartan 6	6	----	0.012
	12.5	----	0.011
	15	----	0.13
	25	----	0.13

6. Results and Discussions.

Fig 9 shows the image of Simulink tool and implementation of proposed work of DC to DC converter and in this image achieved a 50% PWM output. So given input is 10v and for 50% PWM output got a output of 5v. Same is observed in simulation output.

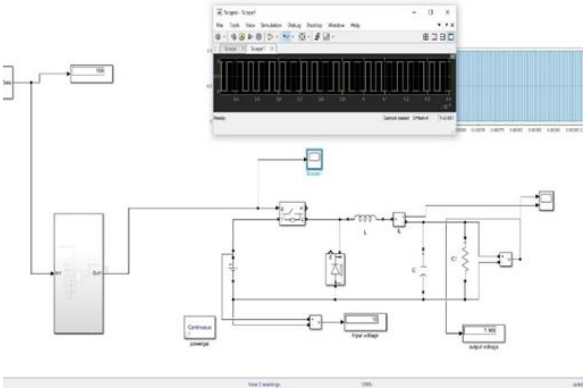

Fig- 9 Waveform of 50% PWM output waveforms.

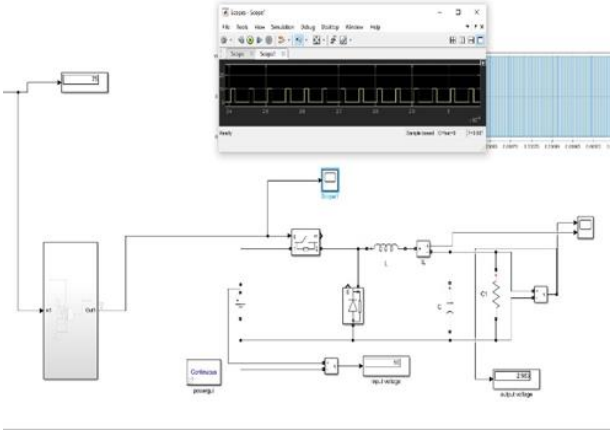

Fig 10 PWM output of 30 percentage Duty cycle.

Above figure 10 shows the digital pulse width modulation(DPWM) implementation in Simulink tool and here proposed design achieved a 30% duty cycle so given input voltage is 10v and the output getting is 2.9v same you can observe in the figure.

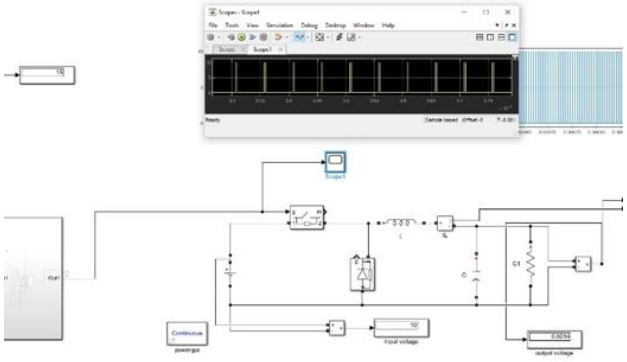

Fig-11 PWM output of 10% Duty cycle

Above diagram shows the output simulation of DPWM of 10% duty cycle. And the applied voltage is 10v and we are able achieve around 0.8v. same can be observed in the figure 11.

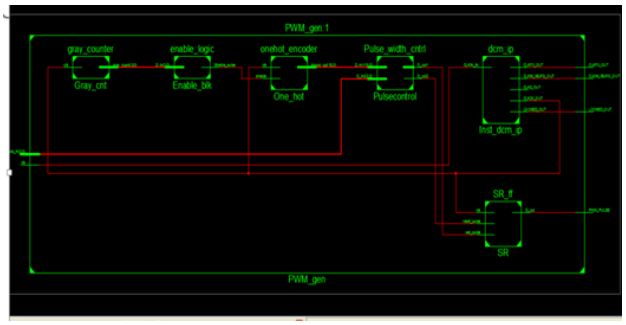

Fig 12- RTL Schematic of PWM architecture.

In Xilinx tool after the checking of the syntax error using check syntax icon, proposed program getting the 0 error means can generate the RTL schematic. Fig 12 shows the diagram of proposed DPWM RTL schematic. RTL schematic consist of Gray counter, one hot encoder, Clk logic, pulse width control block and SR flip flop blocks. Here a single program is written in Verilog code. Verilog code is consist of all required DPWM blocks and same schematic is linked to MATLAB Simulink tool.

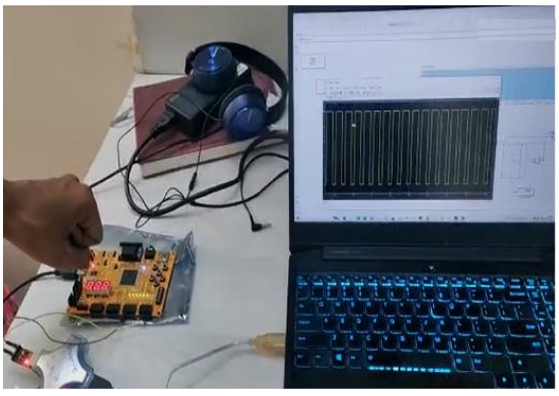

Fig 13- Simulation output in isim having a PWM output of 55%.

Fig 13 shows the digital pulse width modulation of 55%

duty cycle its mentioned as PWM_out and can see the other related waveforms and timing analysis in the above image. Like enable flip flop outputs, one hot encoder related waveforms can be observed in the image.(fig-13).

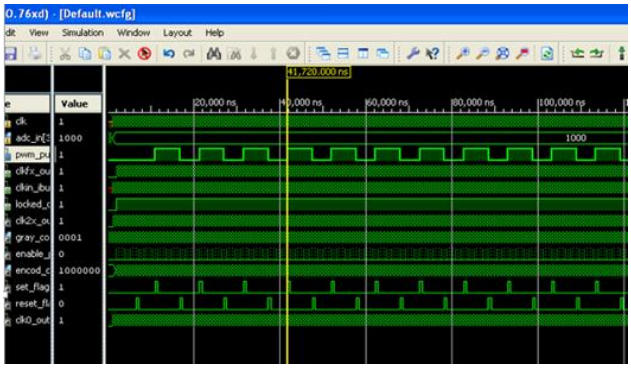

Fig-14 Simulation output in isim having a PWM output of 75%.

Fig 14 shows the digital pulse width modulation of 75% duty cycle its mentioned as PWM_out and can see the other related waveforms and timing analysis in the above image.

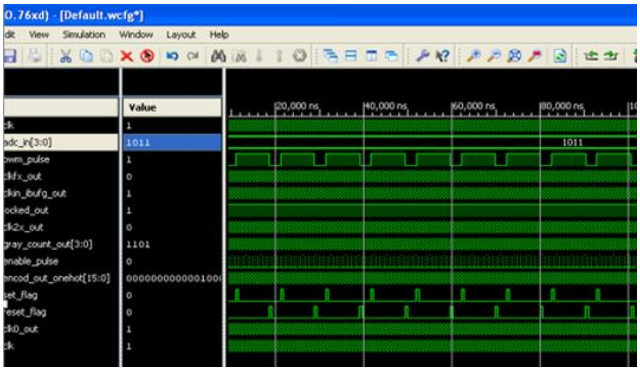

Fig:15 Interfacing of FPGA and observing the output in Simulink tool.

Figure 15 shows the image of interfacing of FPGA block along with MatLab simulink tool and observing the DPWM output in the system. By pressing the key in the FPGA boards we can very the duty cycle as per requirement of the design.

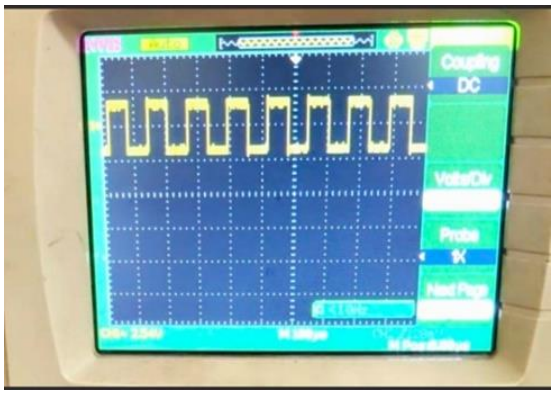

Fig-16 DPWM output for Duty Cycle =50%

Figure 16 shows the image DPWM of duty cycle of 50%.

Whatever observed in Simulink tool by using FPGA block same can be observed in the Digital Storage Oscilloscope by using FPGA hardware.

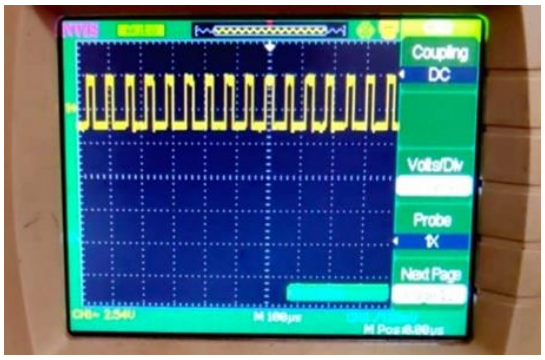

Fig-17 DPWM output for Duty Cycle = 15%

From the FPGA hardware board it passes the waveform for the software in the way of CMOS port it take the reading from the board and in Simulink with the design and show the output in the form of voltage and it varies the waveform in oscilloscope. For example if we set a duty cycle of 15% for an input voltage of 10V then the output voltage will be approximately 1.5V. same can be observed using DSO.

7. Conclusions

This research has achieved the development and simulation of a Gray counter-based PWM architecture for Spartan 6 FPGA board implementation. In contrast to conventional binary counter-based PWM architectures, which are susceptible to glitches and higher power dissipation due to multiple bit changes and the use of comparators, this innovative method utilizes the Gray counter. The Gray counter ensures that only one-bit changes at a time, eliminating the need for a comparator in PWM pulse generation. The architecture is implemented in Verilog code, and simulations are conducted using the ISIM simulator, with integration into Simulink for in-depth analysis. The digital pulse width modulation output is observed in both Simulink and a digital storage oscilloscope, revealing an impressive circuit efficiency of 99%. This highlights its significant value as a component for generating the required voltages in various Software-Defined Radio (SDR) designs.

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