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An Efficient Low-Power Reconfigurable Model For CMOS-Based SRAM Using FPGA

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Abstract: Due to the high-speed communication process in the memory cell, there is a requirement of a high-speed parallel switching operation to enhance the flexibility, reliability and accuracy of the memory cells. To achieve this, a low-power complementary metal oxide semiconductor (CMOS)-based static random-access memory (SRAM) using field programming gate array (FPGA) architecture has been proposed in this paper. High-speed reconfigurable on-chip CMOS SRAM memory blocks are used for optimal utilization of fast and low-power SRAM blocks and have been deployed on the 10T SRAM cells. The proposed method is used to help facilitate fast access to the reconfigurable data bits using Reconfigurable shadow CMOS SRAM Cells. The combined effect of reconfigurable CMOS SRAM cells and shadow SRAM technologies are used to reduce the delay and power by about 8.136 ns and 0.018 W for the 10T SRAM memory cells, as per the simulation result. Due to these phenomena, the area utilization for deployment is higher as compared to conventional methods such as 4T SRAM and 6T SRAM. This has been achieved with the help of FPGA-based CMOS SRAM memory cells.

Keywords: *Complementary metal oxide semiconductor (CMOS), static random-access memory (SRAM), field programming gate array (FPGA), Complex Programmable Logic Devices (CPLDs), Configurable Logic Blocks (CLBs), logical elements (LEs).*

1. Introduction

CMOS (Complementary Metal-Oxide-Semiconductor) technology and nanotechnology have both played crucial roles in advancing reconfigurable architectures in modern computing systems. Reconfigurable architectures refer to designs that can adapt and change their functionality based on the specific tasks or applications they are executing. These architectures offer a balance between the flexibility of software and the efficiency of hardware. The combination of CMOS and nanotechnology enables the creation of more efficient and powerful reconfigurable devices as shown in figure.1. [1]

Modern integrated circuits frequently employ CMOS semiconductor technology. It works perfectly for a variety of gadgets and devices, such as microprocessors, memory chips, and digital logic circuits, because to its low power consumption, strong noise immunity, and ease of integration. In reconfigurable architectures, CMOS technology is being used to build Field-Programmable Gate Arrays (FPGAs) and Complex Programmable Logic Devices (CPLDs). These devices consist of an array of configurable logic blocks and programmable interconnects that allow designers to implement custom digital circuits. By loading different configurations onto these devices, users can change their functionality and tailor them to specific applications [2].

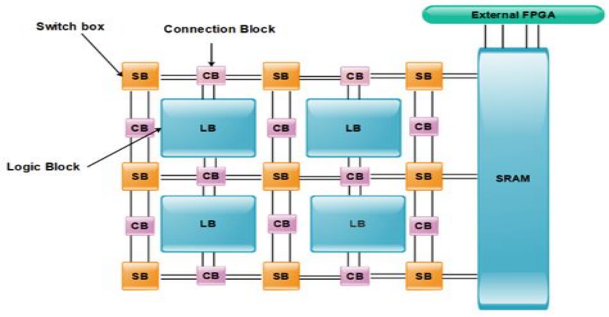

Fig.1 Fundamental block diagram of CMOS based FPGA

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1.1 Nanotechnology*:*

Nanotechnology refers to the manipulation of matter at the nanoscale level, typically involving structures with dimensions between 1 and 100 nanometers. Nanotechnology has opened up new possibilities for

developing smaller, faster, and more power-efficient devices. In the context of reconfigurable architectures, nanotechnology has contributed to the elaboration of nanoscale devices and components perhaps integrated into CMOS technology. Nanoscale transistors and interconnects enable higher transistor densities, reduced power consumption, and improved performance [3].

The combination of CMOS and nanotechnology in reconfigurable architectures has several benefits:

- **Increased Efficiency:** The use of nanoscale components allows for higher transistor density, enabling more complex and efficient reconfigurable devices.
- **Lower Power Consumption:** Nanoscale transistors typically consume less power, leading to energy-efficient reconfigurable architectures.
- **Higher Performance:** Faster switching speeds of nanoscale transistors result in improved performance and faster reconfiguration times.
- **Enhanced Flexibility:** With CMOS-based reconfigurable architectures, users can change the configuration on-the-fly, adapting the device to different computational tasks as needed.
- **Integration:** Reconfigurable architectures constructed on CMOS and nanotechnology can be integrated with traditional microprocessors, memory, and other components, providing a heterogeneous computing platform that combines general-purpose processing with custom hardware acceleration [4].

1.2 Field-Programmable Gate Array (FPGA) architecture usage in digital integrated circuit:

A Field-Programmable Gate Array (FPGA) is a type of reconfigurable digital integrated circuit that is widely utilized in many different applications, such as digital signal processing, hardware acceleration, prototyping, and more. FPGAs are based on CMOS technology and utilize SRAM cells to implement configurable logic elements [5].

Here's an briefing of the FPGA architecture in CMOS SRAM technology:

- Configurable Logic Blocks (CLBs):

Configurable Logic Blocks are primary building blocks of an FPGA.

These blocks are responsible for implementing the desired logic functions based on the configuration data loaded into the FPGA. Each CLB typically contains multiple look-up tables (LUTs), which are small memory arrays used to store the truth table of a specific logic function. The LUTs can be automated to accomplish any logic operation, making the CLBs highly flexible [6].

- Programmable Interconnects:

The CLBs in an FPGA are connected through a network of programmable interconnects. These interconnects consist of routing resources that allow signals to be routed from one CLB to another, forming complex digital circuits. The configuration data specifies how the interconnects should be set up, enabling the FPGA to implement the anticipated logic functions and data paths.

- SRAM Configuration Memory:

The key feature that distinguishes FPGAs from other programmable logic devices is their SRAM-based configuration memory. The configuration data, which defines the functionality of the FPGA, is stored in SRAM cells. When the FPGA is powered up or reconfigured, the configuration data is loaded into the SRAM cells, effectively defining the logical connections and functionality of the CLBs and interconnects. This reconfigurability allows FPGAs to be dynamically changed or programmed for various applications.

- Input/Output Blocks (IOBs):

FPGAs have specialized Input/Output Blocks (IOBs) that serve as interfaces between the internal logic and external devices. The IOBs provide bidirectional I/O functionality, allowing the FPGA to have communication with other digital systems, such as microprocessors, memories, sensors, or communication interfaces.

- Dedicated Hardware Blocks (DSP, RAM, etc.):

Modern FPGAs often include additional specialized hardware blocks, such as Digital Signal Processing (DSP) units and embedded RAM blocks. These blocks are improved for explicit functions and provide enhanced performances applicable in signal processing and data storage.

- Configuration Controller:

The Configuration Controller is responsible for managing the configurable progression. It controls the loading of configurable data from exterior storage (e.g., flash memory) into the SRAM cells, ensuring that the FPGA is correctly programmed with the desired logic and functionality.

CMOS logic and nano RAMs, particularly 10T SRAM are important components in modern electronic devices and computing systems. Let's briefly discuss each of these technologies:

- CMOS Logic:

CMOS logic is a fundamental building block of modern integrated circuits. It is extensively applicable in digital logic circuits, microprocessors, memory chips, and other electronic devices. CMOS logic consists of complementary pairs of p-type and n-type metal-oxide-

semiconductor field-effect transistors (MOSFETs) working composed to procedure logic gates, such as AND, OR, NAND, NOR, and more.

The key compensations of CMOS logic are low power consumption, high noise immunity, and scalability to smaller process technologies. Due to these benefits, CMOS technology has turn out to be the foremost fabrication process for digital integrated circuits.

➢ Nano RAMs:

Nano RAMs denotes to the category of next-generation memory technologies that aim to overcome the limitations of custom memory elements like DRAM and SRAM. These emerging memory technologies promise higher density, faster access times, lower power consumption, and non-volatility (data retention even without power).

Unique and the promising nano RAM technologies is ReRAM- Resistive Random Access Memory, which stores data as resistance states within a nanoscale material. ReRAM offers potential advantages with respect to speed, scalability, and endurance as opposed to traditional memories.

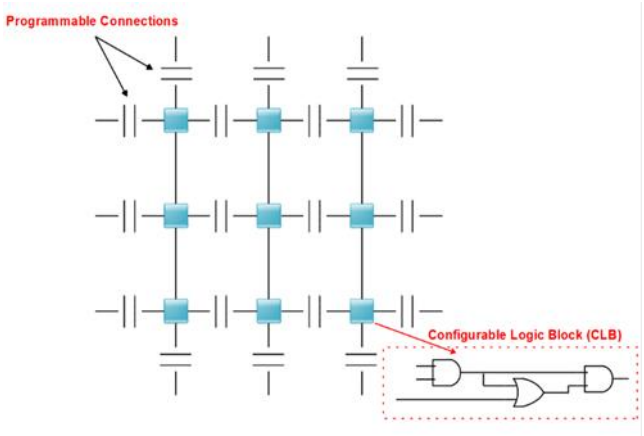


Fig.2 Fundamental FPGA architecture with digital circuit.

➢ 10T SRAM:

SRAM is a type of semiconductor memory that retains data throughout time as it is powered. It is faster and less power-hungry than dynamic RAM (DRAM) but requires more transistors per cell. The basic SRAM cell typically consists of six transistors (6T SRAM) [7][8].

The "10T SRAM" is an alternative SRAM cell design that uses ten transistors, offering improved stability and reduced vulnerability to noise compared to the standard 6T SRAM cell. The additional transistors provide enhanced read and write capabilities, making 10T SRAM suitable for low-power applications and high-density memory designs.

The combination of CMOS logic and nano RAM technologies, such as 10T SRAM, has the capacity to produce more effective and powerful electronic devices with improved memory capabilities. Researchers and engineers continue to explore and develop new technologies that leverage these principles to advance the field of electronics and computing [9][10].

Overall, the combination of CMOS and SRAM-based configuration memory makes FPGAs highly flexible and appropriate for a numerous applications where reconfigurable and high-performance hardware acceleration is required. FPGA designs can be instigated using Hardware Description Languages (HDLs) like Verilog or VHDL, enabling designers to describe complex digital systems that are then synthesized into FPGA configurations [11][12].

1.3 Disadvantage of CMOS SRAM technologies:

While CMOS SRAM has many advantages, It has certain drawbacks as well, which are crucial to take into account for a variety of applications. Here are principle drawbacks of CMOS SRAM:

High Power Consumption: SRAM requires a constant power supply to retain data, as it is a volatile memory. Compared to other memory types like non-volatile memories (e.g., flash memory), SRAM's continuous power requirement makes it less power-efficient, especially in battery-operated devices [13][14].

Larger Area and Higher Cost: The SRAM cell requires multiple transistors (usually six in a basic 6T SRAM cell, and more in more complex variants like 10T SRAM) to store a single bit of data. This higher transistor count results in larger chip area and increased manufacturing costs, making SRAM more expensive compared to dynamic RAM (DRAM) technologies [15][16].

Lower Density: Due to the larger cell size caused by multiple transistors per bit, SRAM has lower memory cell density than DRAM. This implies that SRAM chips have less storage capacity for the same chip area compared to DRAM chips.

Limited Storage Capacity: SRAM's density limitation

makes it impractical for very high-capacity memory applications, such as main memory in modern computers. Instead, it is more commonly used as cache memory or small on-chip buffers due to its fast access times.

Volatility: SRAM is a volatile memory, implies that it loses its stored data when there is no power. This characteristic makes it unsuitable for long-term data storage, unlike non-volatile memories like flash memory or hard disk drives.

Slower Compared to On-Chip Memory: While SRAM is faster than many other memory types, it is still slower than the on-chip registers and cache memories. This speed difference can create latency when transferring data between SRAM and on-chip processing units.

Susceptible to Soft Errors: SRAM is vulnerable to soft errors caused by cosmic rays or high-energy particles, which can disrupt the stored data temporarily. Although error-correcting mechanisms can aid in lessening this problem, it remains a concern in high-reliability applications.

Despite these disadvantages, CMOS SRAM remains a crucial component in modern computing systems, often used as cache memory to bridge the speed gap between high-speed processors and slower main memory. It is also employed in various on-chip buffering and data storage applications where fast access times and low-latency data retrieval are essential. Engineers and researchers continuously work on improving memory technologies To get beyond these restrictions and address the evolving needs of the industry.

1.4 Disadvantage of 10T SRAM technologies:

While 10T SRAM (Static Random-Access Memory) offers certain advantages over the traditional 6T SRAM cell design, it also includes a unique group of disadvantages. Here are some of the key drawbacks of 10T SRAM:

Increased Complexity: The 10T SRAM cell has more transistors than the standard 6T SRAM cell, making it more complex and requiring a larger chip area. This increase in complexity results in higher manufacturing costs and reduced memory cell density, as more space is needed to accommodate each memory cell [17][18].

Slower Access Times: Compared to the 6T SRAM, the 10T SRAM cell typically has slower read and write access times. The additional transistors introduce more capacitance and resistance in the circuit, which can lead to increased access delays.

Higher Power Consumption: The additional transistors in the 10T SRAM cell require more power during read and write operations. This increased usage of power can be a significant disadvantage in low-power and energy-efficient applications [19].

Reduced Bit-Cell Stability: While the 10T SRAM cells provide enhanced stability in comparison to the 6T SRAM, it may still be more vulnerable to certain types of noise and disturbances because of the increased complexity of the cell.

Limited Adoption: While the 10T SRAM cell obsolete studied and proposed as a potential solution to some of the challenges faced by traditional SRAM designs, acceptance of it has been limited in commercial products. The industry has been more inclined towards optimizing 6T SRAM designs or exploring other memory technologies with different trade-offs [20][21].

Process Variability: The additional transistors in the 10T SRAM cell can introduce further process variability, leading to challenges in manufacturing and yield optimization. This variability can impact the reliability and performance of the memory cells.

Design and Verification Complexity: The increased difficulty of the 10T SRAM cell can make the design and verification processes more challenging. It might necessitate more thorough testing and validation efforts, which could lead to longer development cycles [22].

Despite these disadvantages, it's essential to note that the suitability of 10T SRAM depends on specific use cases and design goals. In some scenarios, the benefits it offers in relations to stability and reduced vulnerability to specific kinds of noise might outweigh the drawbacks. However, for general-purpose applications and mainstream memory requirements, designers often opt for more mature and established SRAM cell designs, such as the traditional 6T SRAM, which strikes a balance between performance, power efficiency, and chip area.

Overall, CMOS/nano technology reconfigurable architectures possess the capacity to revolutionize computing systems by providing flexible, energy-efficient, and high-performance solutions for a range of uses, including data centers, edge computing, artificial intelligence, and beyond. As technology continues to advance, we anticipate much more. exciting developments in this field. NATURE technology is a reconfigurable hybrid CMOS/nano architecture that was previously introduced. It may make run-time reconfigurability easier. For the increase of logic density, the NATURE technology employed the concepts of temporal logic folding and fine - grain dynamic reconfiguration using CMOS logic and Nano RAM. The fundamental disadvantage here is the requirement of a fine - grained distribution of nano RAMs across the FPGA architecture. The nano-RAM manufacturing process is not yet mature, so NATURE [23] cannot be used immediately. FPGAs (Field Programmable Gate Arrays)

are future-oriented components that enable flawless hardware customization at a competitive price even in small numbers. Currently available FPGA components are inexpensive and simple to utilise. This makes it an effective factor in reducing costs and time to market when customizing standard products. Integrating application-specific IP cores into FPGAs often avoids time-consuming and costly circuit board redesigns. This is a future alternative, especially when only using small or medium-sized devices [24] for extremely specialized applications. Long-term availability is another crucial factor Another important aspect is long-term availability. Benefits of FPGAs and their near-unlimited availability is that the code doesn't change as devices move from generation to generation. FPGAs contains a logic blocks, a hierarchical structure of programmable logic gate elements, and reconfigurable interconnects that enable the wiring of the blocks. Memory elements, which can be complete memory blocks or arrays of basic flip-flops, are also included in logic blocks. FPGAs have more area, power, and delay factors than application-specific integrated circuits (ASICs), which is one of its disadvantages [25]. This disadvantage is mainly brought on by the extra work required for reconfigurability. To overcome the shortcomings of his current FPGAs, a reconfigurable hybrid CMOS/nanotechnology architecture called NATURE [26] was previously suggested to solve his two main problems: Logic density and runtime reconfiguration efficiency. This NATURE technology is built with Nano RAM and CMOS logic. Due to their high speed and density, these nano-RAMs are helpful because they enable the idea of temporal logic folding, relating to the idea of temporal pipelines [27]. Its disadvantage is the immaturity of manufacturing technology, as well as the need for fine-grained distributed Nano RAM, which increases cost and makes design complex. This FPGA architecture eliminates the drawbacks of nano-RAM and therefore an excellent alternative to nano-RAM with the practice of CMOS logic and devices. Power savings may be accomplished by using low-power 10 T SRAM blocks without recharging. This allows the user to save configuration bits [28], which minimizes bit line charge/precharge power for read instructions [29]. With the suggested 10T SRAM-based FPGA architecture, consumption of power and reconfiguration latency are minimized. As stated by the simulation results, performance has significantly improved because of less latency and competitive power usage. The following fragment of the document is structured as follows: The previous NATURE design is shown in Section II, along with some basic information about the 4T, 6T, and 10T SRAM cells. The suggested architecture based on SRAM is described in Section III and Section IV compares 4T, 6T, and 10T SRAM cells with experimental results on delay and Regarding the energy usage of the suggested architecture utilising 10T SRAM cells. This paper is concluded in Section V.

1. FUNDAMENTAL FACT

The foundational information required to comprehend CMOS SRAM-based NATURE is providing in the following section. The 4T SRAM cell's structure and properties are defined in Section II-A. The structure and features of the 6T SRAM cell are then designated in Section II-B, and the design and properties of the 10T SRAM cell suggested in [4] are defined in Section II-C. The fundamental building elements of memory blocks within the LBs of the FPGA are these 10T SRAM cells, allowing for less power consumption. Section II-D then introduces the concepts behind the NATURE technology [30].

2.1 4 T SRAM

4T SRAM," which stands for 4-Transistor Static Random-Access Memory. SRAM is a kind of semiconductor memory that holds onto information as long as the circuit is powered on. It is commonly used as cache memory in CPUs and other high-speed processing units because of its fast access times and ability to retain data without the need for frequent refreshing [31].

The "4T" in 4T SRAM refers to the number of transistors used in each memory cell. The basic unit of SRAM is a memory cell, which stores a single bit of data. The components of the 4T SRAM cell are four transistors: two access transistors and two cross-coupled inverters.

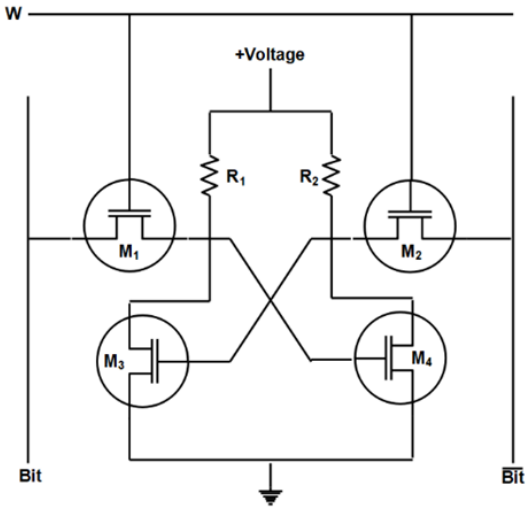


Fig .3 Fundamental structure of 4T SRAM.

According to Figure 3, the circuit comprises of two poly load resistors and four NMOS transistors. Pass transistors are the two NMOS transistors. The gates of these transistors are linked to word lines, connecting the cells to columns. The flip-flop inverters' pull-downs are the other two NMOS transistors. The inverter load consists of very high resistance polysilicon. This cell only requires space for four NMOS transistors [12 Compared to 6T and 10T cells, 4T SRAM cells may be smaller, but Slower speed and higher power consumption[32].

2.2 6 T SRAM

"6T SRAM" stands for 6-Transistor Static Random-Access Memory. It is another type of SRAM cell that is commonly used in modern semiconductor memory designs, particularly in cache memory and high-performance integrated circuits. The 6T SRAM cell is more robust and reliable than the 4T SRAM cell, but Increased area and power consumption are a consequence of it. The usage of CMOS flip-flops is another cell design that gets beyond the earlier mentioned limitation. A PMOS transistor is used in this instance to replace the load. According to Figure 4, this SRAM cell has six transistors: two NMOS transistors attached to the row line, one NMOS and Each inverter requires a single PMOS transistor. Compared to the 4T construction, this cell performs better in terms of speed and power [33]. Due to the absence of readout inverters, this cell construction has a smaller size but uses more power and has a longer latency than a 10T SRAM cell.

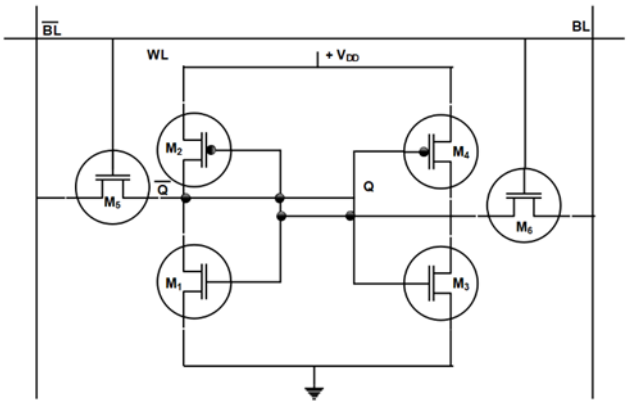


Fig.4 Fundamental structure of 6T SRAM.

2.3 10 T SRAM

Each memory cell in the suggested architecture is comprised of 10T low-power, no-precharge SRAM cells. A standard 6 T SRAM cell, the read-out inverter, and a read-out port for the transmission gate make up a 10T SRAM cell, as depicted in Figure 5. These 10 T SRAM cells allow both read and write operations. Similar to traditional 6T SRAM cells, the write procedure is the same as well. For reads, this 10T SRAM cell uses a non-precharge scheme [30]. It is not necessary for a precharge scheme because the read inverter can fully charge and discharge the read bit line. Therefore, readout power is saved because the bit line voltage remains unchanged until the read-out datum changes. Due to its reduced duration precharge

time, delay is also improved in comparision to traditional

4 T and 6 T SRAM cells. The area required for the cell is very large compared to traditional 6T SRAM cells and 4T SRAM cells. The 10 T SRAM design minimises heavy switching activity on the memory read bit lines and conserves the majority of charge / precharge power, making it for low power applications.

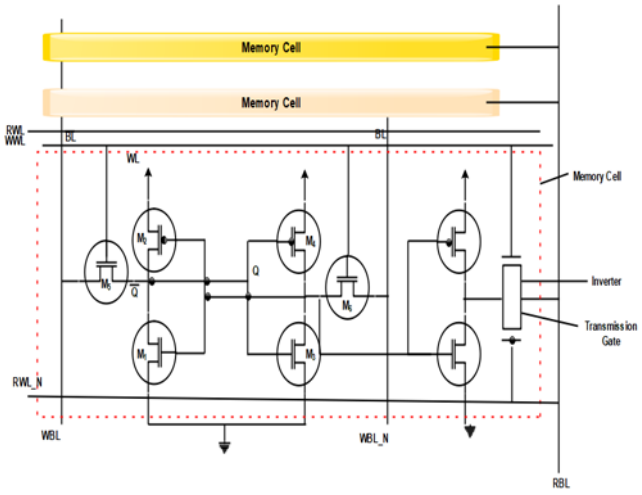


Fig. 5 Fundamental structure of 10 T SRAM cell.

2.4 NATURE

NATURE technology is a reconfigurable hybrid CMOS/nanotechnology architecture in a previous article, facilitates reconfiguration at runtime [30]. This controls nano RAM's reconfiguration bits access. Because accessing the nano-RAM reconfiguration bits has a low latency, the temporal logic convolution is applied. By breaking up a large circuit into numerous smaller convolution stages, logical folding is accomplished. The configuration bits for these levels of convolution are in on-chip nano-RAM employed here. Each cycle modifies the logic and interconnects by loading a fresh configuration from the nano-RAM into the SRAM cells. Note that NATURE delivers significantly higher logic densities, higher power consumption, and competitive latency for large-scale applications. However, we must switch out nano-RAM for SRAM or integrated DRAM in order to realise NATURE technology. The suggested concept examines how employing SRAM affects both delay and power characteristics [30].

The NATURE architecture demands Nano RAMs, which are effective with regard to low power and speed consumption, for each block design. However, this is limited by the single fact that the nano-RAM manufacturing process is not yet mature, which means the design process is difficult. Therefore, we prefer not to use nano RAMs and instead rely on CMOS devices[31].

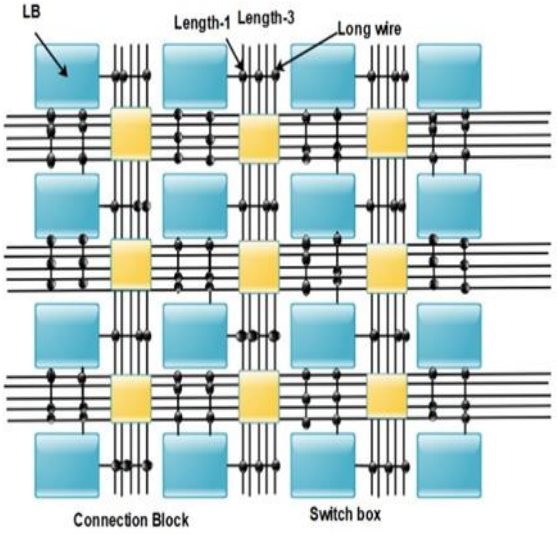


Fig.6 Internal view of SRAM

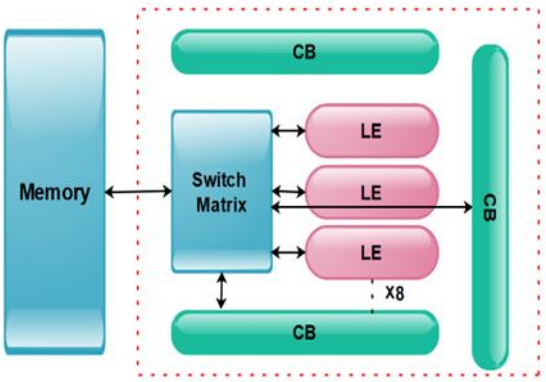


Fig.7 Fundamental architecture of SRAM

2. SRAM Based Architecture

This section introduces the proposed CMOS-SRAM-based NATURE. Figure.6 shows Internal view of SRAM and Figure.7 shows the Fundamental architecture of SRAM. It has island-style LBs connected at various connection levels. The input and output terminals of each LB are connected to the interconnect network by Connection Blocks (CBs) and Switch blocks (SBs), respectively. To support rapid runtime reconfiguration, each Logical block (LB) is mapped to a local 10 T SRAM block that stores configuration copies. Below are details on LB, connectivity, and reconfiguration support.

3.1 Logical blocks (LB)

The FPGA fabric is a two-dimensional array of these configurable logical blocks, often denoted to as "logic cells" or "logic elements." Each logical block consists of a cluster of lookup tables (LUTs), flip-flops, and other circuit elements that is programmable to perform various combinational and sequential logic functions. An array of LBs makes up the FPGA (Field Programmable Gate Arrays) design. According to Figure 8, each of these LBs contains one local switch matrix and eight logical elements (LEs). These LEs in the LB each carry out the required logical calculations [30].

This LB's local switching matrix is intended to enable fast local communication between LEs. The LE has 6 inputs, selected by a switching matrix. With signals coming from the LB's 40 common inputs and 16 feedback signals (two feedback signals per LE), the local switch matrix is intended to function as a 56-to-1-bit multiplexer (MUX). Choose [32]. CB connects the local switch matrix to 40 common inputs, coming from connection network outside LB. CBs and interconnection networks are covered in Section III-C in additional detail.

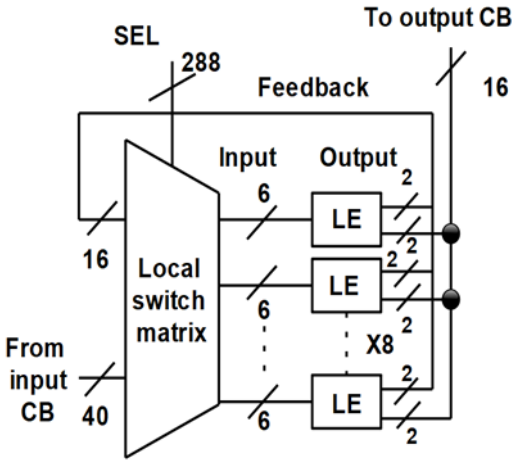


Fig.8 Fundamental design of an LB.

3.2 Logical elements (LE)

Each LB consists of eight LEs that perform the required computations. Figure 9 shows the structure of an LEs containing a 4-input LUT, four D-type flip flops (DFFs) and some crossbars. In contrast with traditional FPGA designs, ours has four DFFs in each LE. When doing logical convolutions, these DFFs are utilized to store numerous temporary computational results, easing communication between stages.

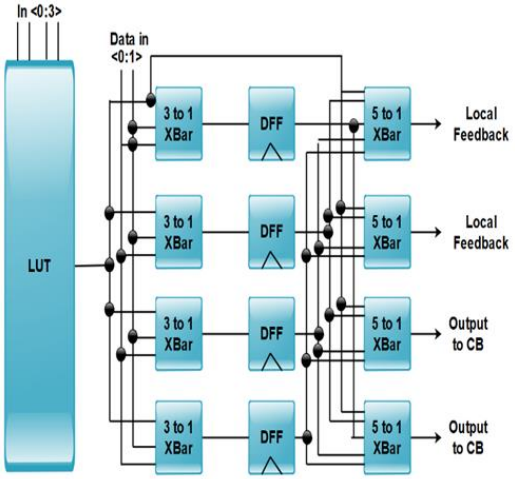


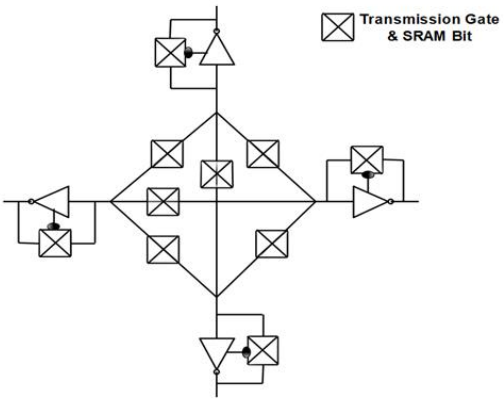
Fig.9 Fundamental design of an LE

The 5-to-1 crossbar chooses the LE output signal either from LUT or DFF, while the 3-to-1 crossbar chooses the signal to latch. On the basis of designated select lines, the 3-to-1 and 5-to-1 crossbars function as switches and select signals. The other LE outputs [30] are supplied back to the local LEs through switch matrix. Other two LE outputs are connected to the interconnection network via CB and are a component of the LB output.

3.3 Interconnects

Connections and routing between individual elements within the LB are done to facilitate communication between stages.

(a)



(b)

Fig .10 Switch Block Architecture (a) Switch Block (b) Switch design.

A routing architecture is needed to enable logical folding and effective local communication while preserving high area efficiency. The connection architecture comprises of wired portion at different levels, CBs, and SBs. The LB has 16 outputs and 40 common inputs. These have connection with a network of connection with the help of transmission gates. Figure 10(a) shows switch box, which has each pin connected to SB. The control box has 32 switches in it. The switch design suggested in [31] can be observed in figure 10(b). Transmission gates connect pairs of tracks, and every SB output has an output buffer. The area efficiency is improved by using four buffers for six connections. The transmission gates, acting as buffers connect the tracks to vertical track. Communication between the horizontal and vertical directions is made

possible by these links. This switching matrix is solely utilised in this architecture as a multiplexer to choose inputs according to the specific lines employed in each logic component of the FPGA architecture's logic block [31]. This lowers average power and lowers latency, enabling effective reconfiguration.

3.4 The support in decrease reconfiguration delay

The key component of this architecture's dynamic reconfigurability is predicated on quick access to reconfiguration bits within embedded memory. The foundation of the suggested design is a low-power, high-speed 10T RAM that supports wide bit widths and faster read operations. However, there is a latency overhead associated with loading the reconfiguration bits from the local memory block each cycle. Therefore, we added a shadow SRAM cell to each reconfigurable element to further enhance performance and hiding reconfiguration delays. such as.

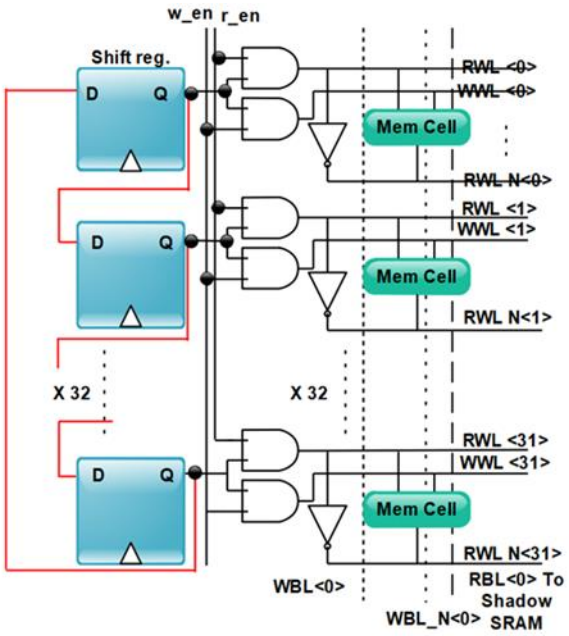


Fig.11 Proposed Memory block's read circuit configuration.

Each LB in Figure 6 is associated to a 10 T SRAM block. Copies of LB, CB, and SB's configuration are kept in this SRAM block. 32 different FPGA-mapped circuit configurations can be stored in this memory. In order to hold 32 Configuration bits, memory blocks must be used. Figure 11 illustrates the implementation of a shift register made up of 32 DFFs connected in series, which activates 32-word lines (each with 1438 bits) each row. The read bit line (RBL) in figure 8 is used to supply the shadow SRAM with configuration high-speed 10T RAM [31][32] that supports wide bit widths and faster read operations.

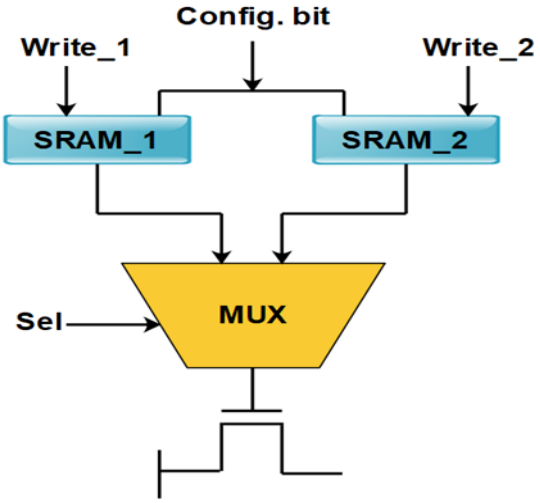


Fig.12 Proposed Shadow SRAM.

However, there is a latency overhead associated with loading the reconfiguration bits from the local memory block each cycle. Therefore, we added a shadow SRAM cell to each reconfigurable element to further enhance performance and hiding reconfiguration delays. such as. Each LB in Figure 6 is connected to a 10 T SRAM block. Copies of LB, CB, and SB's configuration are kept in this SRAM block. 32 different FPGA-mapped circuit configurations can be stored in this memory. In order to hold 32 Configuration bits, memory blocks must be used. Figure.11 illustrates the implementation of a shift register made up of 32 DFFs connected in series, which activates 32-word lines (each with 1438 bits) each row. The read bit line (RBL) in Figure 12 is used to supply the shadow SRAM with configuration information. A traditional FPGA uses only one of his SRAM cells for controlling reconfigurable switches. Latency overhead is increased by accessing a local 10T SRAM block for reconfiguration. We employ the shadow SRAM approach described in [33] to conceal this delay. Figure.11 demonstrates how this method performs for reconfigurable switch control. It comprises of a 2:1 MUX and 6T SRAM cells, two in number. The signals, write1 and write2, of the SRAM1 and SRAM2 cells are fed by the WBL and WBL_N signal lines from the read circuitry. Sel signal chooses the switch controlling signal for current cycle. While one SRAM is in usage, the other SRAM has to be constructed to perform computation or kept in Wait state if the first cell is used in the succeeding cycle. Therefore, the composition delay can be completely hidden if the memory access time is faster than the computational delay [34].

3. Results and Discussions

This section presents the results of simulation for the suggested architecture, with 10T SRAM cells for each memory cell in the read circuit of memory coupled to the logic blocks. In general, increasing the level of folding generally results in more LBs and less latency. We can demonstrate how adopting a shadow SRAM method minimizes the delay during reconfiguration, though, since we are just building a single logic block for the FPGA architecture [34][35]. In comparison to 4 T and 6 T SRAM cell structures designs based on CMOS SRAM, various aspects of the proposed design will have an impact on the parameters of area, a delay and performance. First, in comparison to single standard SRAM cell, there is increase in area by the addition of shadow SRAM cells. In Shadow SRAM, configuration delays are hidden behind computation delays. Second, 10T CMOS-based SRAM cells utilize CMOS technology, but at the cost of larger area, lower latency and lower performance. Compared to nano-RAM, 10T SRAM has higher storage space overhead [36]. In traditional FPGAs, connectivity accounts for majority of the power consumption. The fact that logical folding uses more power with more connections, reduces power consumption. Increasing the level of folding does not significantly increase the number of overall connections, but reduces the additional routing complexity of intra-level communication. Designers must choose the right technology to meet their particular application and product requirements to avoid trade-offs between performance, latency, and area. It is determined that the non-precharge SRAM cell approach is the only way to reduce power[36][37][38]. When comparing the capabilities of 4 T, 6 T, and 10 T SRAM cells, it is evident that each of them has distinguished features that enhance area, delays, and power.

TABLE 1 Area, delay and power comparison between 4T, 6T and10T SRAM cell

LOGIC UTILIZATION	**SRAM cell Structures**		
	4T SRAM	**6T SRAM**	**10T SRAM**
DELAY	9.049 ns	8.924 ns	8.035 ns
POWER	0.089 W	0.081W	0.015W

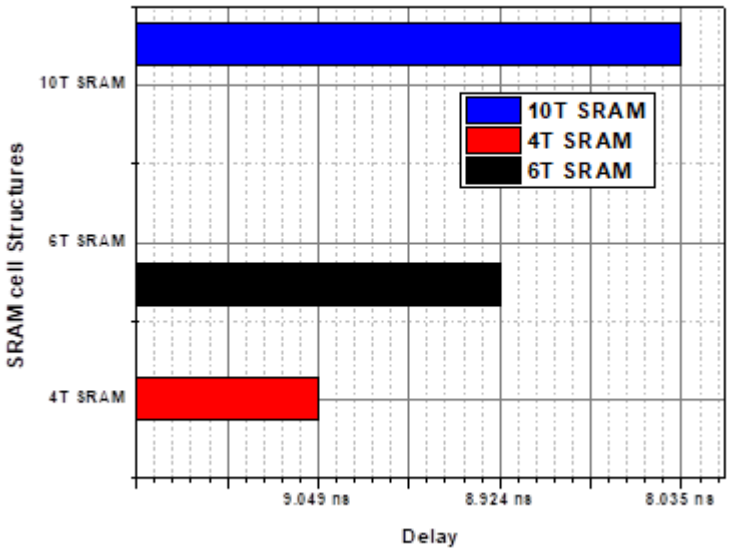


Fig .13 comparison analysis between conventional method with proposed method with respect to the delay

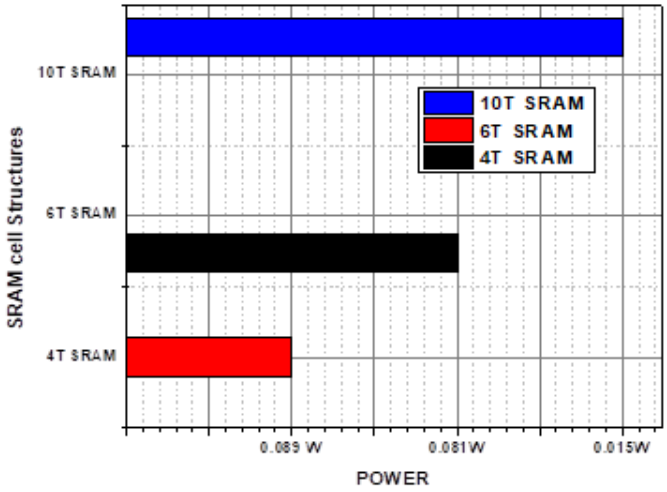


Fig.14 comparison analysis between conventional method with proposed method

TABLE 2 Area, delay and power tradeoffs of LB employed with 10T SRAM cell in Memory Block

SRAMCELL	AREA	DELAY	POWER
10 T SRAM	239	8.979 ns	0.052 W

consumption parameters. As can be seen, the delay in reconfiguration can be minimized by quickly accessing the Memory Block configuration bits. Also, latency and power factors can be reached at slower rates because there is a small overhead in space. When using 10T SRAM,

memory space overhead rises from 10.6% when using nano-RAM [38] to 26.3%. This allows tradeoffs between latency and performance. However, if we perform logical folding, we find that the power-delay product exhibits the same pattern as the delays for various folding levels. This is because power adjustments are minor in comparison to delay changes. Simulation work was performed on the SPARTAN 3E family of Xilinx design suite 14.2 Version

using XC3S250E device in the FT256 package [39][40][41][42]. Table 1 shows comparative results for 4 T, 6 T, and 10 T SRAM cells that can be employed in this architecture and its comparison analysis as revealed in Figure.13 and Figure.14 From the comparison results, we can conclude that 6T and 10T have lower latency and average power consumption than 4T. However, the 10 T SRAM cell has significantly lower latency and power usage in comparison to two other SRAM designs with area overhead. These drawbacks can be minimised by using fast and low power 10 T SRAM cells in the LB of the proposed design architecture, which helps reduce delays during reconfiguration. Therefore, employing 10 T SRAM cells in the proposed architecture ensures effective performance with excellent design flexibility.

Table 2 displays the LB's area, latency, and power trade-offs when each memory cell is used with a 10 T SRAM cell in the proposed FPGA design. By comparing the specifications of 4 T, 6 T, and 10 T SRAM cells, it is observed the 10 T SRAM cell performs significantly better in terms of minimizing both latency and consumption of power [9]. The 10 T SRAM does not need a precharge circuit because it has a readout inverter, and because the Shadow SRAM uses two SRAM cells, the delay of the configuration bits during reconfiguration is much decreased. The 10T SRAM design is a good contender for wide on-chip memory for low-power applications because it avoids excessive switching activities on memory read bit lines and hence saves the majority of charge/precharge power [42]. To improve the LB's performance, we therefore use 10T SRAM cells in each of its memory cells, which are tabulated as shown in Table 2.

4. Conclusion

The work has combination of CMOS SRAM-based logic blocks and CMOS logic in FPGA architecture. This framework uses low power 10 T blocks of his SRAM as storage elements for configuration bits. In comparison to traditional 4 T and 6 T SRAM cells with area overhead, the 10T SRAM cell's non-precharge approach shortens precharge time, lowering consumption of power and latency. Shadow SRAM technique can entirely mask configuration delays because memory access times are quicker than computational delays. A LB design using 10 T SRAM cells is simulated in XILINX ISE design suite 14.2 with a SPARTAN 3E family and XC3S250E target device. 4 T, 6 T and 10 T performance analysis is done using the TANNER tool. According to simulation results, the power usage can be reduced from about 0.089W (for 4T) to 0.015W (for 10T) and from 0.081W (for 6T) to 0.015W (for 10T), improving LB performance to do. The reconfiguration delay is also shortened from roughly 9.049ns (for 4 T) to 8.035ns (for 10 T) and 9.049 ns (for 6 T) to 8.035 ns (for 10 T). This architecture offers tremendous design flexibility by allowing different trade-offs between area, latency, and power usage.

Future memory cell strategies for the LB may employ 12 T SRAM cells to further reduce delay and increase performance, and implemented using C2MOS logic low power technique can also be used to achieve power savings.

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Author contributions

Rekha Sathyanarayana Gowda[1]: Conceptualization, Methodology, Software and Editing, Nataraj Kanathur Ramaswamy[2]: Data curation, Writing-Original draft preparation, Software, Validation. Rekha Kanathur Ramaswamy[3] Writing-Reviewing.

References

[1] Y. Zhou, S. Thekkel and S. Bhunia, "Low power FPGA design using hybrid CMOS-NEMS approach," Proceedings of the 2007 international symposium on Low power electronics and design (ISLPED '07), Portland, OR, USA, 2007, pp. 14-19, doi: 10.1145/1283780.1283785.

[2] V. K. Joshi and S. Borkar, "A comparative study of NC and PP-SRAM cells with 6T SRAM cell using 45nm CMOS technology," 2016 International Conference on Advances in Electrical, Electronic and Systems Engineering (ICAEES), Putrajaya, Malaysia, 2016, pp. 58-62, doi: 10.1109/ICAEES.2016.7888009.

[3] Kyomin Sohn et al., "An autonomous SRAM with on-chip sensors in an 80nm double stacked cell technology," Digest of Technical Papers. 2005 Symposium on VLSI Circuits, 2005., Kyoto, Japan, 2005, pp. 232-235, doi: 10.1109/VLSIC.2005.1469374.

[4] Soon-Moon Jung et al., "A study of formation and failure mechanism of CMP scratch induced defects on ILD in a W-damascene interconnect SRAM cell," 2001 IEEE International Reliability Physics Symposium Proceedings. 39th Annual (Cat. No.00CH37167), Orlando, FL, USA, 2001, pp. 42-47, doi: 10.1109/RELPHY.2001.922879.

[5] A. Bhaskar, "Design and analysis of low power SRAM cells," 2017 Innovations in Power and Advanced Computing Technologies (i-PACT),

Vellore, India, 2017, pp. 1-5, doi: 10.1109/IPACT.2017.8244888.

[6] P. S. Kanhaiya, C. Lau, G. Hills, M. D. Bishop and M. M. Shulaker, "Carbon Nanotube-Based CMOS SRAM: 1 kbit 6T SRAM Arrays and 10T SRAM Cells," in IEEE Transactions on Electron Devices, vol. 66, no. 12, pp. 5375-5380, Dec. 2019, doi: 10.1109/TED.2019.2945533.

[7] Uk-Rae Cho et al., "A 1.2-V 1.5-Gb/s 72-Mb DDR3 SRAM," in IEEE Journal of Solid-State Circuits, vol. 38, no. 11, pp. 1943-1951, Nov. 2003, doi: 10.1109/JSSC.2003.818137.

[8] Nam-Seog Kim, Yong-Jin Yoon, Uk-Rae Cho and Hyun-Geun Byun, "Programmable and automatically adjustable on-die terminator for DDR3-SRAM interface," Proceedings of the IEEE 2003 Custom Integrated Circuits Conference, 2003., San Jose, CA, USA, 2003, pp. 391-394, doi: 10.1109/CICC.2003.1249425.

[9] J. H. Jang et al., "A 2.05 um/sup 2/ full CMOS ultra-low power SRAM cell with 0.15 nm generation single gate CMOS technology," International Electron Devices Meeting 2000. Technical Digest. IEDM (Cat. No.00CH37138), San Francisco, CA, USA, 2000, pp. 579-582, doi: 10.1109/IEDM.2000.904386.

[10] H.. -S. Yu et al., "A SRAM Core Architecture with Adaptive Cell Bias Scheme," 2006 Symposium on VLSI Circuits, 2006. Digest of Technical Papers., Honolulu, HI, USA, 2006, pp. 128-129, doi: 10.1109/VLSIC.2006.1705343.

[11] Sang-Hun Seo et al., "Effects of gate notching profile defect on characteristic of cell NMOSFET in low-power SRAM device," 2003 8th International Symposium Plasma- and Process-Induced Damage., Corbeil-Essonnes, France, 2003, pp. 146-149, doi: 10.1109/PPID.2003.1200944.

[12] S. Patil and V. S. K. Bhaaskaran, "Optimization of power and energy in FinFET based SRAM cell using adiabatic logic," 2017 International Conference on Nextgen Electronic Technologies: Silicon to Software (ICNETS2), Chennai, India, 2017, pp. 394-402, doi: 10.1109/ICNETS2.2017.8067966.

[13] K. J. Kim et al., "A novel 6.4 /spl mu/m/sup 2/ full-CMOS SRAM cell with aspect ratio of 0.63 in a high-performance 0.25 /spl mu/m-generation CMOS technology," 1998 Symposium on VLSI Technology Digest of Technical Papers (Cat. No.98CH36216), Honolulu, HI, USA, 1998, pp. 68-69, doi: 10.1109/VLSIT.1998.689202.

[14] Sang-Hun Seo et al., "A novel double offset-implanted source/drain technology for reduction of gate-induced drain-leakage with 0.12-μm single-gate low-power SRAM device," in IEEE Electron Device Letters, vol. 23, no. 12, pp. 719-721, Dec. 2002, doi: 10.1109/LED.2002.805769.

[15] H. Sato et al., "A 5-MHz, 3.6-mW, 1.4-V SRAM with nonboosted, vertical bipolar bit-line contact memory cell," in IEEE Journal of Solid-State Circuits, vol. 33, no. 11, pp. 1672-1681, Nov. 1998, doi: 10.1109/4.726557.

[16] W. -G. Ho, K. -S. Chong, T. T. -H. Kim and B. -H. Gwee, "A Secure Data-Toggling SRAM for Confidential Data Protection," 2020 IEEE International Symposium on Circuits and Systems (ISCAS), Seville, Spain, 2020, pp. 1-1, doi: 10.1109/ISCAS45731.2020.9180698.

[17] S. K. K, K. P. B, V. M and R. K. R. D V, "A Design of Low Power Full Seu Tolerance RHBD 10t Sram Cell," 2020 IEEE India Council International Subsections Conference (INDISCON), Visakhapatnam, India, 2020, pp. 27-32, doi: 10.1109/INDISCON50162.2020.00018.

[18] I. Alouani, H. Ahangari, O. Ozturk and S. Niar, "NS-SRAM: Neighborhood Solidarity SRAM for Reliability Enhancement of SRAM Memories," 2016 Euromicro Conference on Digital System Design (DSD), Limassol, Cyprus, 2016, pp. 154-159, doi: 10.1109/DSD.2016.12.

[19] C. -W. Wu, M. -H. Chang, C. -C. Chen, R. Lee, H. -J. Liao and J. Chang, "A configurable 2-in-1 SRAM compiler with constant-negative-level write driver for low Vmin in 16nm Fin-FET CMOS," 2014 IEEE Asian Solid-State Circuits Conference (A-SSCC), KaoHsiung, Taiwan, 2014, pp. 145-148, doi: 10.1109/ASSCC.2014.7008881.

[20] P. Sharma, R. Anusha, K. Bharath, J. K. Gulati, P. K. Walia and S. J. Darak, "Quantification of figures of merit of 7T and 8T SRAM cells in subthreshold region and their comparison with the conventional 6T SRAM cell," 2016 20th International Symposium on VLSI Design and Test (VDAT), Guwahati, India, 2016, pp. 1-2, doi: 10.1109/ISVDAT.2016.8064899.

[21] Soon Moon June, Sung Bong Kim, Jung Sup Uom, Won Suek Cho, Joo Young Kim and Kyung Tae Kim, "High density low power full CMOS SRAM cell technology with STI and CVD Ti/TiN barrier metal," ICVC '99. 6th International Conference on VLSI and CAD (Cat. No.99EX361), Seoul, Korea (South), 1999, pp. 119-121, doi: 10.1109/ICVC.1999.820842.

[22] A. S. V. S. V. P. D. Kumar, B. S. Suman, C. A. Sarkar and D. V. Kushwaha, "Stability and

Performance Analysis of Low Power 6T SRAM Cell and Memristor Based SRAM Cell using 45NM CMOS Technology," 2018 International Conference on Recent Innovations in Electrical, Electronics & Communication Engineering (ICRIEECE), Bhubaneswar, India, 2018, pp. 2218-2222, doi: 10.1109/ICRIEECE44171.2018.9009119.

[23] T. Seki et al., "A 6-ns 1-Mb CMOS SRAM with latched sense amplifier," in IEEE Journal of Solid-State Circuits, vol. 28, no. 4, pp. 478-483, April 1993, doi: 10.1109/4.210031.

[24] M. Chaturvedi, M. Garg, B. Rawat and P. Mittal, "A Read Stability Enhanced, Temperature Tolerant 8T SRAM Cell," 2021 International Conference on Simulation, Automation & Smart Manufacturing (SASM), Mathura, India, 2021, pp. 1-5, doi: 10.1109/SASM51857.2021.9841199.

[25] Hansraj, A. Chaudhary and A. Rana, "Ultra Low power SRAM Cell for High Speed Applications using 90nm CMOS Technology," 2020 8th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO), Noida, India, 2020, pp. 1107-1109, doi: 10.1109/ICRITO48877.2020.9197869.

[26] J. K. Mishra, H. Srivastava, P. K. Misra and M. Goswami, "A 40nm Low Power High Stable SRAM Cell Using Separate Read Port and Sleep Transistor Methodology," 2018 IEEE International Symposium on Smart Electronic Systems (iSES) (Formerly iNiS), Hyderabad, India, 2018, pp. 1-5, doi: 10.1109/iSES.2018.00011.

[27] C. -H. Yu, P. Su and C. -T. Chuang, "Impact of Random Variations on Cell Stability and Write-Ability of Low-Voltage SRAMs Using Monolayer and Bilayer Transition Metal Dichalcogenide (TMD) MOSFETs," in IEEE Electron Device Letters, vol. 37, no. 7, pp. 928-931, July 2016, doi: 10.1109/LED.2016.2564998.

[28] A. Priadarshini and M. Jagadeeswari, "Low power reconfigurable FPGA based on SRAM," 2013 International Conference on Computer Communication and Informatics, Coimbatore, India, 2013, pp. 1-6, doi: 10.1109/ICCCI.2013.6466160.

[29] S. Yadav, Y. Bansal, B. Joseph and R. K. Kavitha, "Low-Power Dual-Vt 7T SRAM Bit-Cell With Reduced Area and Leakage," 2022 IEEE Delhi Section Conference (DELCON), New Delhi, India, 2022, pp. 1-5, doi: 10.1109/DELCON54057.2022.9753131.

[30] M. Li, P. Wu, B. Zhou, J. Appenzeller and X. S. Hu, "Cross-Coupled Gated Tunneling Diodes With Unprecedented PVCRs Enabling Compact SRAM Design—Part II: SRAM Circuit," in IEEE Transactions on Electron Devices, vol. 69, no. 11, pp. 6085-6088, Nov. 2022, doi: 10.1109/TED.2022.3207122.

[31] S. Gupta, K. Gupta and N. Pandey, "Performance evaluation of SRAM cells for deep submicron technologies," 2016 Second International Innovative Applications of Computational Intelligence on Power, Energy and Controls with their Impact on Humanity (CIPECH), Ghaziabad, India, 2016, pp. 292-296, doi: 10.1109/CIPECH.2016.7918785.

[32] M. Bansal, A. Kumar, P. Singh and R. K. Nagaria, "A Novel 10T SRAM cell for Low Power Applications," 2018 5th IEEE Uttar Pradesh Section International Conference on Electrical, Electronics and Computer Engineering (UPCON), Gorakhpur, India, 2018, pp. 1-4, doi: 10.1109/UPCON.2018.8596829.

[33] H. Banga and D. Agarwal, "Single bit-line 10T SRAM cell for low power and high SNM," 2017 International Conference on Recent Innovations in Signal processing and Embedded Systems (RISE), Bhopal, India, 2017, pp. 433-438, doi: 10.1109/RISE.2017.8378194.

[34] Y. Kim, Q. Tong, K. Choi and Y. Lee, "Novel 8-T CNFET SRAM cell design for the future ultra-low power microelectronics," 2016 International SoC Design Conference (ISOCC), Jeju, Korea (South), 2016, pp. 243-244, doi: 10.1109/ISOCC.2016.7799768.

[35] H. Okamura, T. Saito, H. Goto, M. Yamamoto and K. Nakamura, "Mosaic SRAM Cell TEGs with intentionally-added device variability for confirming the ratio-less SRAM operation," 2013 IEEE International Conference on Microelectronic Test Structures (ICMTS), Osaka, Japan, 2013, pp. 212-215, doi: 10.1109/ICMTS.2013.6528174.

[36] R. Deena Kumari Selvam, C. Senthilpari and L. Lini, "Low power and low voltage SRAM design for LDPC codes hardware applications," 2014 IEEE International Conference on Semiconductor Electronics (ICSE2014), Kuala Lumpur, Malaysia, 2014, pp. 332-335, doi: 10.1109/SMELEC.2014.6920865.

[37] M. U. Mohammed, A. Nizam and M. H. Chowdhury, "Performance Stability Analysis of SRAM Cells Based on Different FinFET Devices in 7nm Technology," 2018 IEEE SOI-3D-Subthreshold Microelectronics Technology Unified Conference (S3S), Burlingame, CA, USA, 2018, pp. 1-3, doi: 10.1109/S3S.2018.8640161.

[38] M. U. Mohammed and M. H. Chowdhury,

"Reliability and Energy Efficiency of the Tunneling Transistor-Based 6T SRAM Cell in Sub-10 nm Domain," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, no. 12, pp. 1829-1833, Dec. 2018, doi: 10.1109/TCSII.2018.2874897.

[39] V. Rukkumani, M. Saravanakumar and K. Srinivasan, "Design and analysis of SRAM cells for power reduction using low power techniques," 2016 IEEE Region 10 Conference (TENCON), Singapore, 2016, pp. 3058-3062, doi: 10.1109/TENCON.2016.7848609.

[40] N. Surana and J. Mekie, "Energy Efficient Single-Ended 6-T SRAM for Multimedia Applications," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 1023-1027, June 2019, doi: 10.1109/TCSII.2018.2869945.

[41] R. Kumar et al., "Design and Benchmark of Iso-Stable High Density 4T SRAM cells for 64MB arrays in 65nm LSTP," 2020 IEEE 17th India Council International Conference (INDICON), New Delhi, India, 2020, pp. 1-7, doi: 10.1109/INDICON49873.2020.9342091.

[42] G. Prasad, B. c. Mandi, P. Ramu, T. V. Sowrabh and A. H. Kumar, "Statistical Analysis of 5T SRAM Cell for Low Power and Less Area SRAM Based Cache Memory for IoT Applications," 2020 First International Conference on Power, Control and Computing Technologies (ICPC2T), Raipur, India, 2020, pp. 368-372, doi: 10.1109/ICPC2T48082.2020.9071468.

[43] B. V. Garidepalli, R. Prasad Somineni, A. Peddi and U. M. Janniekode, "Design and Analysis of 16nm GNRFET and CMOS Based Low Power 4kb SRAM Array Using 1-Bit 6T SRAM Cell," 2022 IEEE IAS Global Conference on Emerging Technologies (GlobConET), Arad, Romania, 2022, pp. 102-108, doi: 10.1109/GlobConET53749.2022.9872358.