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# Concurrent Computation Strategies: Unveiling the Power of Vedic Mathematics

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**Abstract:** Within the dynamic realm of computational techniques, the fusion of age-old wisdom with contemporary technology has emerged as an intriguing frontier. This endeavor involves a profound investigation that combines the ancient wisdom of Vedic Mathematics with modern computing concepts. This innovative expedition not only reinvigorates conventional mathematical methodologies but also reveals the unexplored capabilities of simultaneous computation. The study presents the design and statistical analysis of a concurrent vedic multiplier architecture, suitable for various parallel computing applications, utilizing contemporary concurrent hardware architectures. This research study focuses on the multiplier architecture, which is the most hardware-intensive component. The ideas of Vedic mathematics are employed to define this architecture. The multiplier's architecture is explained using the basic principles of Very High-Speed Integrated Circuit Hardware Description Language (VHDL). The architecture is developed utilizing the latest High-Level Synthesis (HLS) Tool, such as Xilinx Vivado 2018.2. The architecture is designed to cater to various types of FPGA, including general-purpose, automotive, military, and high-reliability environments. Its primary objective is to ensure exact control over crucial characteristics such as delay, frequency, resources, and power..

***Keywords*:** *Vedic Mathematics, Virtex, Kintex, Artix, VHDL.*

## 1. Introduction

In order to fulfil the societal needs, almost every day, smart products are thought of and are developed using top-notched technology. Such revolutionary products are outcome of the foundations like Signal Processing, Artificial Intelligence, Image Processing, Cloud Computing.

Big Data Processing and similar other tools; and the products are always expected to be super quick, highly responsive, reliable, small in size and most significantly utilizes least power. On the other side of the coin, all of these applications use complex mathematical procedures, which are hardware intensive. Out of different complex mathematical computations, which are prominently used in the development of the smart products, one of the mathematical components that is multiplier architecture is designed and developed using fundamentals of vedic mathematics.

Vedic mathematics is the short-cut technique structured for handling the complex mathematical applications using pen and paper.The fundamentals of the vedic mathematics are configured around “16 formulas and 13 sub-formulas”. Out of these formulas and sub-formulas, Urdhav- Tiryagbhyam formula is used for implementation of the multiplier component. This component is implemented using the concepts of concurrent hardware architecture like “Field Programmable Gate Arrays” (FPGA). The architecture of the component is described using VHDL and the design is targeted to the diverse variations of the FPGA like Virtex, Kintex and Artix. Further, to get the precise estimation of the sententious parameters like delay, frequency, resource and power, in case if the designed multiplier component is applied to diverse applications, the custom estimations are done for general purpose, automotive, military or critical applications and low voltage applications. The said architecture is simulated to perform the logical verification of the architecture. Further the architecture is synthesized and implemented using Xilinx Vivado 2018.2 High Level Synthesis tool for hardware verification. Through the subsequent sections of the research paper, literature review, fundamentals of the vedic mathematics, implementation and outcome at various stages are disclosed.

## 2. Literature Review

In digital system, computation of arithmetic operations such as multiplication and division are obtained by performing consecutive addition and subtraction for a specific number of times. A multiplier circuit is used to perform the multiplication of two binary numbers. A multiplier is also known as binary multiplier, it is constructed using adder circuits. The computational speed of the system relies on the adders utilized. Different

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realization of adders is employed to enhance the computational speed of the multiplier carry adder. In the present research work, the authors [1] have proposed the Vedic multiplier structures with dissimilar carry look-ahead adders such as “factorized regular, block”, “regular, and factorized block carry look-ahead adder”. Primarily the Vedic multiplier was realized “employing regular carry look-ahead adder” and substitute with “advance adders”.

In digital signal processing, multiplier and accumulator unit is the fundamental element. In designing a chip, it is necessary to think about some design constraints like power, region, and delay. Furthermore, a proficient multiplier and adder unit has an important role in determining the performance speed of multiply and accumulate. The paper [2] proposed the design of a 16 bit multiply and accumulate unit utilizing a 16-bit Vedic multiplier. The Vedic multiplier is developed by using the concept of the UrdhavTiryakbhyam sutra. The proposed multiplier when compared with the traditional 16-bit Vedic multiplier contains carry save adders, the outputs show that there is an improvement in delay by 32% and improvement in power by 24%.

In computer, “Reduced Instruction Set Computer” (RISC) is a microprocessor central processing unit design with extremely optimized commands, minimum and dedicated command rules that are not found in the structure of Complex Instruction Set Computer (CISC). Reduced Instruction Set Computer has been optimized with a great number of registers and a command pipelining and permits a small number of clock cycles per instruction. In the paper [3], a 16 bit RISC processor design is proposed that can execute a large number of instructions. The authors used Vedic Sutras to perform arithmetic logic unit and multiplier and accumulator. The main challenging task in Vedic mathematics is to diminish the complex calculations of traditional techniques and to simplify them. The proposed Reduced Instruction Set Computer processor is capable of performing 15 instructions simultaneously. The Vedic multiplier and accumulator and arithmetic logic unit are integrated with the “control unit, register bank, program counter and memory blocks to develop a 16-bit Vedic processor”.

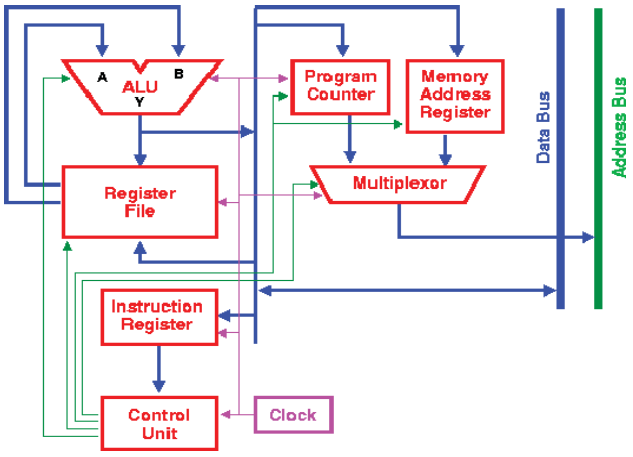


**Fig. 1.** Block diagram of a processor

A multiplier is an electrical circuit used in digital systems, such as central processing units, to perform the multiplication of binary values. It is created using binary adders. Various computer arithmetic techniques can be employed to implement a digital multiplier. The Vedic multiplier is a very efficient digital multiplier with minimal delay time. The construction of the Vedic multiplier closely resembles that of the array multiplier, with certain alterations made to the most critical bit. Among the “16 Vedic sutras”, “UrdhavTiryagbhyam” stands out as the method for multiplication that may be universally applied. The time delay is directly proportional to the number of multiplication bits. The authors suggested implementing a very efficient Vedic multiplier. The Vedic multiplier implementation is achieved using a Very high-speed integrated circuit hardware description language. The architecture is designed by structural modelling way using components like adders, AND gates, and OR gates. [4] The effectiveness of the arithmetic modules influenced high-speed digital signal processing applications. Multiplication and division have more complex computation operations than other arithmetic operations. Vedic mathematics gives an easy technique of execution as these methods are based on the principles on which human intelligence works. The authors [5] proposed a novel scalable structure for Paravartya in which eight fractional proportion terms are produced in every step and generate a proportion that is precise up to a single decimal digit. When the proposed structure is compared with the

existing traditional structure it is found that it is 4.5 nanoseconds faster than the conventional implementation of the Paravartya sutra.

In quantum-dot cellular automata technology, square computation also known as self-multiplier using Vedic mathematics is new learning which attracts many new researchers. The authors [6] proposed the "coplanar quantum-dot cellular automata structure" for 2 bits square computation utilizing "Urdhva Tiryagbhyam" Vedic sutra. In addition, an optimized structure is proposed which is based on XOR gate and majority gate. The optimized structure demonstrates prominent improvement compared with the conventional structures. It requires a smaller amount of cells, a smaller region and lower latency. Furthermore, there is an improvement in terms of power dissipation as the proposed quantum-dot cellular automata structure dissipates less power than the similar type complementary metal oxide semiconductor structure design.

In Digital signal processing applications, a "finite impulse response filter" of 45-nanometer technology is a basic filter. In this paper, the authors proposed a design and evaluation of a finite impulse response filter of 45 nanometres using Vedic mathematics. To design such a finite impulse response filter, the authors also employed a Vedic multiplier and D type register. For the computational information comparison, 4 bit 2 taps direct and transposed form of finite impulse response filter has been designed. The experimental outputs show that the proposed finite impulse response filter has six times lower power consumption than the traditional filters. The number of delay elements used for the design of finite impulse response filter decreases power consumption, region and number of transistors. The proposed design improves the overall performance and decreases the power consumption of finite impulse response has been enhanced considerably. [7]

Vedic multiplier plays an important role in various digital signal processing applications. Depending upon how the data is handled, Vedic multiplies are organized in upheld manner. The design complexity of the integrated circuit is growing as the technology enhanced in very large- scale integrated leads to the accumulation of the number of elements on a single integrated circuit. As the integrated circuit has a high concentration, the power dissipated in the integrated circuits results in the low power complementary metal oxide semiconductor very large-scale integrated designs. Complex multiplication is one of the essential computation processes in digital computer systems and digital signal processing techniques. The authors [8] review the 2*2 Vedic multiplier processes utilizing several low-power and high-speed adders.

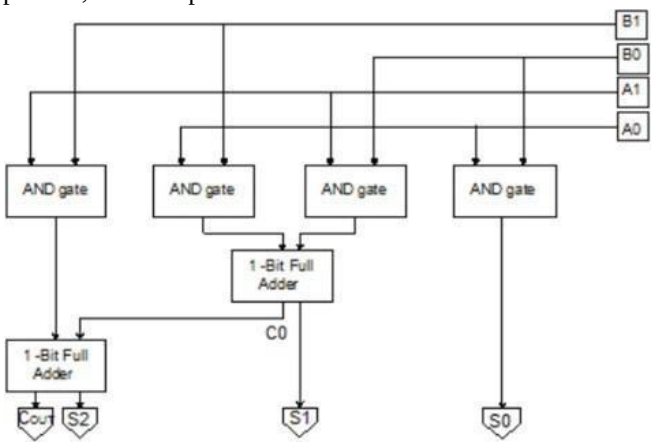


**Fig. 2.** Structure of 2*2 multiplier

QCA is an ingenious nano rank evaluation technology that suggested smaller proportions like less power utilization and less region related to the complementary metal oxide semiconductor designing method. Modern digital computerization always focuses on higher concentration and very low power utilization. A Vedic multiplier plays an important role in many digital circuit's applications like digital signal processing. The authors in [9] have designed ultra-efficient and less complicated multipliers by using quantum-dot cellular automata XOR gate and less complicated quantum-dot cellular automata half adder. An efficient four-bit ripple carry adder is also designed using quantum-dot cellular automata designer simulation circumstances for less energy and high- speed nanotechnology applications. The experimental output shows that the proposed design run faster than the traditional designs within the condition of cell assessments, region and latency.

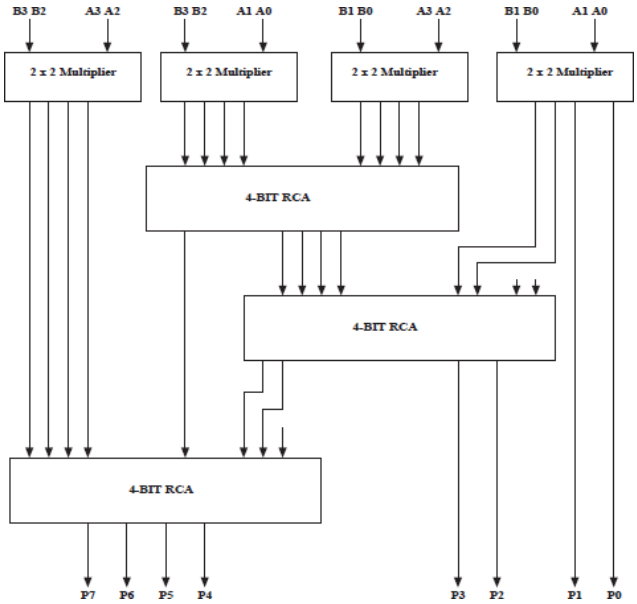


**Fig. 3.** Block diagram of QAC 4*4 multiplier

Effective multiplier structure is essential as this process has acquired key importance in digital processing applications like filter designs. Developing such high-speed multipliers with low power and less delay is necessary for this constraint. The proposed research investigation [10] is based on metrics such as region, power dissipation and speed. Insufficient power Very large-scale integrated structures refer to methods and procedures specifically developed to reduce the overall power consumption of an integrated chip. Estimating the use of low power structural design is expected to reduce power consumption in advanced devices with high integration density, hence enhancing operational speed. The redundant binary representation technique is utilized to optimize the power and area efficiency of the Vedic 8x8 multiplier architecture. The “UrdhvaTiryakbhyam” Sutra, which extends Vedic algorithms to include signed numbers, has been implemented. The proposed structure yields superior power outputs compared to existing architectures..

The system gives better performance if the time taken by the multiplier for computation is less. Nowadays, the multiplier is defined as which consumes power at a similar instance speed of multiplier is playing very important aspects. During the selection of multiplier, adders like carry look ahead adder, carry skip adder and ripple carry adder plays an important role. In the paper [11], the authors have compared the transmission gate technique and complementary metal oxide semiconductor technique with mass systems with several adders. The experimental results show some variations in the power factors like a 20% decrease in average power, energy delay product decreases to great extent for CLA.

In India, the term Veda is defined as an unimpeded library of all knowledge. Out of the four upavedasthapatya contains all kinds of architectural and structural human effort. Vedic mathematics is a keepsake given to human beings by ancient sages. Vedic mathematics makes all the complex arithmetic calculations simple when compared with modern days mathematics. The need for fast speed in today's modern day is met by digital multipliers. Multipliers are crucial components in a wide range of high-speed devices, as they perform complex multiplication operations by repeatedly squaring a value. In Vedic mathematics, Yavadunam is one of the finest squaring algorithms. In this paper, the authors proposed a squaring structural design by realizing the Yuvadunam algorithm. Xilinx software is utilized for the simulation and realization of the proposed design. [12]

Multiplying one number with another number is known as one kind of arithmetic operation. In digital signal processing, multiplication operation plays an important role in several applications like linear convolution, Fast Fourier transforms, and arithmetic logic unit of the microprocessor. For digital systems, it is essential to design a multiplier with lessened delay and proficient power consumption. This paper proposed a 64-bit arithmetic logic unit design based on Vedic sutras like Nikhilam and UrdhvaTiryagbhyam. Field programmable gate arrays are employed for execution. The proposed Vedic multiplier gives outputs after computation in 4 nano-second time. The authors used the Xilinx field-programmable gate arrays tool for realizing the arithmetic logic unit module. [13]

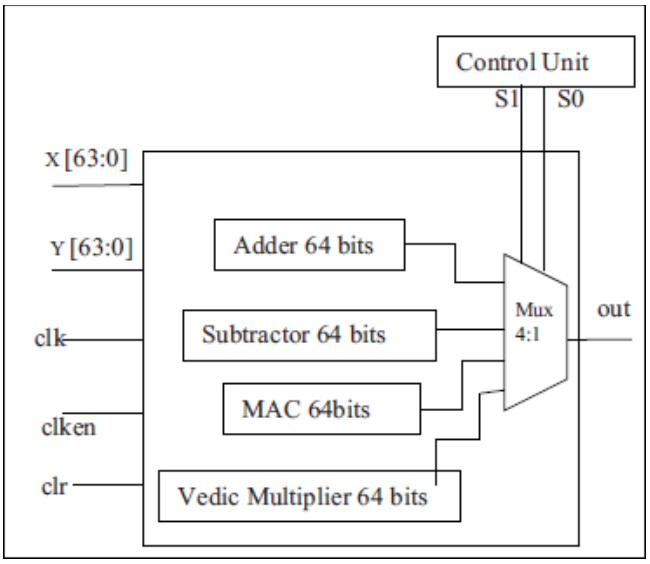


**Fig. 4.** Block diagram of 64 bits Arithmetic model

The term multiplication means performing an addition operation of the partial products. This repeated operation performed by the processor is defined by its speed. In digital signal processing applications, the speed of the multiplication and power efficiency of the multiplier has greater significance. In India, Traditional mathematics is the oldest method of mathematics that provides results based on sutras. Vedic mathematics sutra is a powerful tool to perform complex mathematical operations like multiplication. Out of 16 sutras in Vedic mathematics, UrdhavaTiryagbhyam provides proficient in realizing multiplication. In any microprocessor, the speed of the processor depends on the performance of its multiplication. Several structural designs are proposed for realizing multiplier but multiplier based on Vedic mathematics outputs in high- speed calculation. [14]

## 3. Fundamentals of Vedic Mathematics

Vedic mathematics is the tactics proposed to execute the complex mathematical computations in much easy and faster way using pen and paper. These tactics can be used to solve complex calculations in the sections of "Arithmetic, Plain and Co-ordinate Geometry, Trigonometry, Quadratic Equations, Factorization and Calculus". The outcome of using the vedic principles is in the form of execution in easy steps and in promising time. The vedic fundamentals are designed around "16 sutras" (formulas) and "13 up-sutras" (Sub-formulas), as stated through the following Table Iand Table II along with their meaning.

**TABLE I. 16** VEDIC SUTRAS

| Sr. No. | Formula | Meaning |
|---|---|---|
| 1. | (Anurupye) | If one is in ratio, the |

| S. No. | Formula | Meaning |
|---|---|---|
| 1 | Shunyamanyat | "other is zero" |
| 2. | Chalana-Kalanabyham | "Differences and Similarities" |
| 3. | EkadhikinaPurvena | "By one more than the previous One" |
| 4. | EkanyunenaPurvena | By one less than the previous one |

| | | |
|---|---|---|
| 5. | Gunakasamuc hyah | "The factors of the sum are equal to the sum of the factors" |
| 6. | Gunitasamuch yah | "The product of the sum is equal to the sum of the product". |
| 7. | NikhilamNava tashcaramamD ashatah | "All from 9 and last from 10" |
| 8. | ParaavartyaYojayet | "Transpose and adjust" |
| 9. | Puranapuranabyham | "By the completion or Noncompletion" |
| 10. | Sankalana-vyavakalanabh yam | "By addition and by subtraction" |
| 11. | ShesanyankenaCharamena | "The remainders by the last digit" |
| 12. | ShunyamSaamyasamuccaye | "When the sum is the same that sum is zero" |
| 13. | Sopaantyadvayamantyam | "The ultimate and twice the penultimate" |
| 14. | Urdhva-tiryakbhyam | "Vertically and crosswise" |
| 15. | Vyashtisamanstih | "Part and Whole" |
| 16. | Yaavadunam | Whatever the extent of its deficiency. |

**TABLE II.** 13 VEDIC SUB-SUTRAS

| S. No. | Formula | Meaning |
|---|---|---|
| 1. | Anurupyena | "Proportionately" |
| 2. | SisyateSesasmjnah | "The remainder remains constant" |
| 3. | Adyamadyenant yamantyena | "The First by the first and the last by the last" |
| 4. | KevalaihSaptakamGunyat | "For 7 the multiplicand is 143" |

| | | |
|---|---|---|
| 5. | Vestanam | "By Osculation" |
| 6. | YavadunamTavadunam | "Lesses by the Deficiency" |
| 7. | YavadunamTav dunamVarganc aYojayet | "Whatever the deficiency lessens by that amount and set up the square of the Deficiency" |
| 8. | Antyayordasake'pi | "Last Totaling 10" |
| 9. | Antyayoreva | "Only the last terms" |
| 10. | Samuccayagunitah | "The sum of the Products" |
| 11. | Lopanasthapana bhyam | "By alternate elimination and Retention" |
| 12. | Vilokanam | "By mere observation" |
| 13. | Gunitasmuccaya hSamuccayagun itah | "The product of the sum is the sum of the products" |

The field of vedic mathematics consists of a set of "16 primary formulae". Among these options, there are only 5 formulas provided for conducting multiplications. These can be further categorized as the individual technique and the general or universal technique of multiplication. A particular way of multiplication can be employed when certain conditions are met, such as when both numbers are close to 100, when the numbers are in close proximity to each other, or when the sum of the last digits of the numbers is 10. On the other hand, the general or universal technique of multiplication can be used in any situation. The table below presents the vedic formulas utilized for multiplication, along with their corresponding meanings.

**TABLE III.** VEDIC FORMULAS FOR MULTIPLICATION

| S. No. | Formula | Meaning | Technique |
|---|---|---|---|
| 1. | Nikhilam Sutra | All from 9 and last from 10 | Specific |
| 2. | Anurupyena Sutra | Proportionately | Specific |
| 3. | Ekayunena Purvena | By one less than the previous one | Specific |
| 4. | Antyaordas ke'pi | Last Totaling 10 | Specific |

| | | | |
|---|---|---|---|
| 5. | UrdhavTiry agbhyam | Vertically and crosswise | **Generic** |

*A. Nikhilam Sutra*

The Nikhilam formula is employed to multiply numbers that are close to powers of 10, such as 99 and 96, 999 and 992, 103 and 104, 999 and 1004, and so on. It is a specialized method of multiplication that is employed to multiple numbers that are close to a power of 10. This method involves three distinct scenarios:

• Numbers that are smaller and closer to a power of 10.

• Numbers that are larger and closer to a power of 10.

• Numbers that are in close proximity to and situated on both sides of a power of 10.

*B. Anurupyena Sutra*

The Nikhilam Sutra is a mathematical technique employed for multiplication when the number in question is not in close proximity to a power of 10, but rather closer to itself. The execution process begins by establishing a working base, which is then followed by the application of the Nikhilam sutra.

*C. Ekayunena Purvena*

EkayunenaPurvena trick of multiplication in vedic mathematics is applicable whenever the multiplier consists of 9's. This trick deals with three possibilities arising, which are:

- Number of digits in multiplicand and multiplier are same.
- Number of digits in multiplicand are more than multiplier.
- Number of digits in multiplier are more than multiplicand.

*D. Antyaordaske'pi*

This technique of Vedic multiplication is utilized when the sum of the least significant numbers is equal to 10. The following steps can be utilized to perform multiplication. This technique involves verifying that the sum of the least significant digits of the multiplicand and multiplier is equal to 10.If the sum is 10, then multiply the least significant digits to obtain the second half of the result. Additionally, add 1 to the remaining digits and multiply them by the original digit.

*E. Urdhav Tiryagbhyam*

The "UrdhavTirygbhyam" method is a universal approach to performing multiplication for any amount of digits, unlike other methods that are specialized to certain cases. The formula "UrdhavTirgbhyam" is a universal formula that can be used for all multiplication scenarios. This methodology is employed to execute the suggested framework. When employing this formula for multiplication, the multiplication can be started from either the left side or the right side. To perform multiplication using the "UrdhavaTirgbhyam" Method, begin with the leftmost digit of both the 3-digit multiplicand and multiplier.:

- Vertical multiplication of 1st digits of multiplicand and multiplier.
- Crosswise multiplication of the first two digits and addition of the intermediate multiplication result.
- Crosswise multiplication of first and last digits of multiplicand and multiplier; Vertical multiplication of 2nd digits of multiplicand and multiplier; Addition of intermediate multiplication results.
- In all steps, except first one, each digit position of the result must have only one digit, if not, then carry forward to the next digit position.

Example-II:

1 4 5

3 7 3

---

[(1x3) | (1x7) + (4x3) | (1x3) + (5x3) + (4x7) | (4x3) + (5x7) | (5x3)]

**TABLE IV.** EXAMPLE-I OF URDHAV-TIRYAGBHYAM METHOD

| Example-1:<br><br>1 2 3<br><br>4 5 6<br><br>----------<br><br>[(1x4) \| (1x5) + (2x4) \| (1x6) + (3x4) + (2x5) \| (2x6) + (3x5) \| (3x6)] |
|---|

**TABLE V.** EXAMPLE-II OF URDHAV-TIRYAGBHYAM METHOD

## 4. Implementation

Using the above steps, 32x32 vedic multiplier architecture is designed. The process of verification begins with the logic verification. In this step, the known set of input values are applied to the component under test and output response is observed. If the output responses are closer to the expected one, the component under test is concluded to be ok. Otherwise, the component is modified. Such verification, at the early stage, assures quick time to market.

In early days of the development, the constructs of the VHDL were designed for simulation purposes only. With the passage of time, the language is also used for synthesis. But since it was developed for simulation purpose only, all the VHDL statements can not be converted in to equivalent hardware structure. Hence, to verify whether the architecture is perfectly converted into hardware architecture or not, the component is synthesized.Soon after, the architecture is implemented. In this process, tiny steps like place, map and routing are done. With the usage of most recent HLS tool like Xilinx Vivado, precise estimation of the crucial parameters like delay, frequency, resource and power can be done, without architecture being actually been implemented into the hardware.

In the subsequent section, the outcome of the model is discussed through different steps.

### *A. Logic Verification*

The outcome of the simulation process is discussed through the Fig.5 to Fig.8.

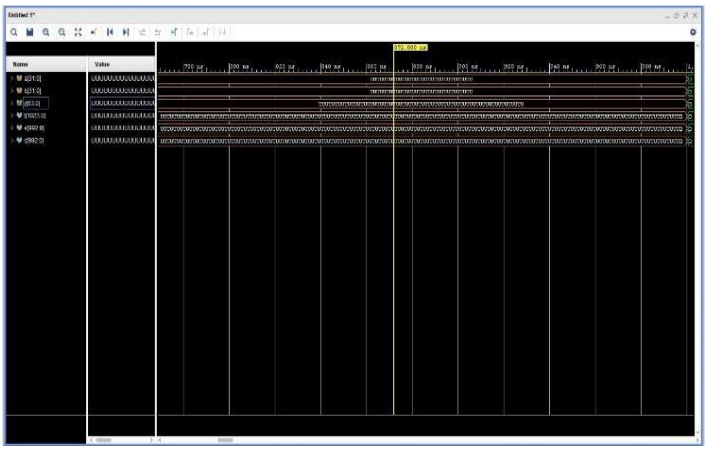

**Fig. 5.** Simulation View (1)

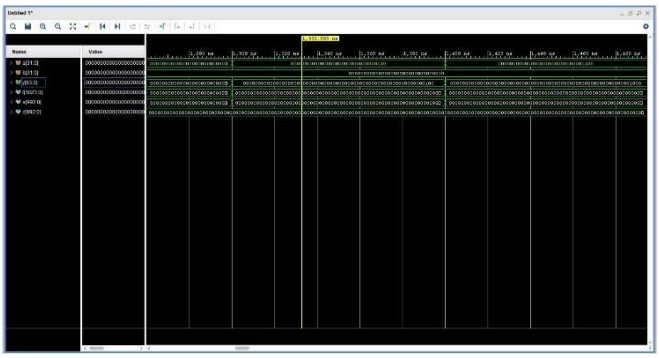

**Fig. 6.** Simulation View (2)

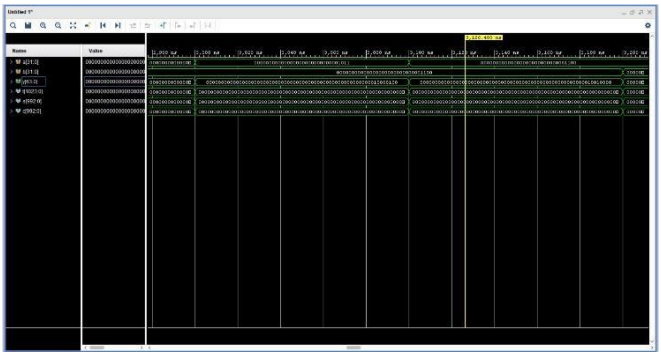

**Fig. 7.** Simulation View (3)

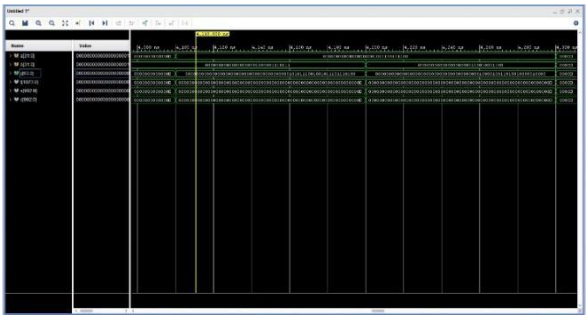

**Fig. 8.** Simulation View (4)

*B. Synthesis*

RTL view is the means through which we can visually inspect like which components are used for implementation of the described component. This pictorial analysis is carried out through RTL schematic step in HLS tools. This process can be done in two steps as Pre-Synthesis view and Post Synthesis view. The pre-synthesis view is the general architecture development without targeting the HDL description to any specific device. Whereas, the Post-Synthesis view indicates the precise utilization of the component by targeting the description to the specific device technology. Through the subsequent section, the RTL view (Pre-Synthesis and Post-Synthesis) are disclosed.

- RTL Schematic (Pre-Synthesis):

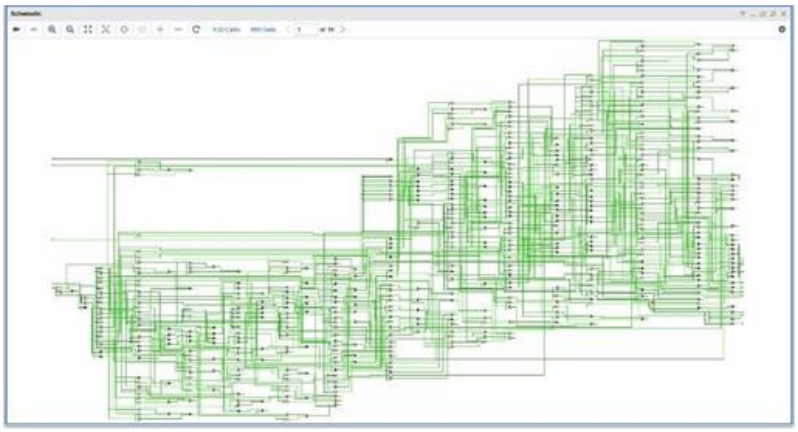

**Fig. 9.** RTL Schematic (Pre-Synthesis) View (1)

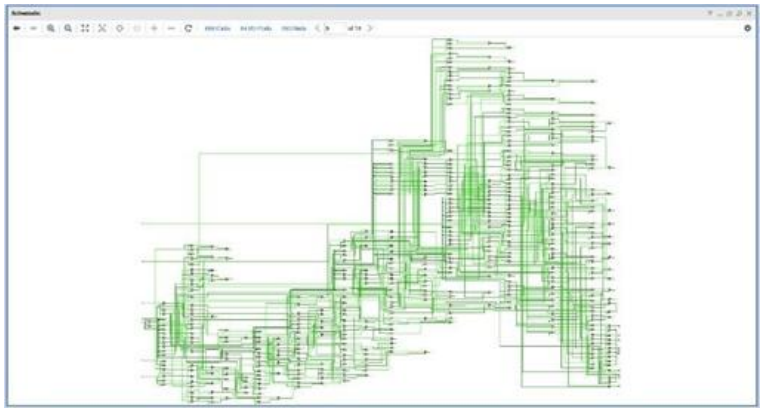

**Fig. 10.** RTL Schematic (Pre-Synthesis) View (2)

**Fig. 11.** RTL Schematic (Pre-Synthesis) View (3)

- RTL Schematic (Post-Synthesis)

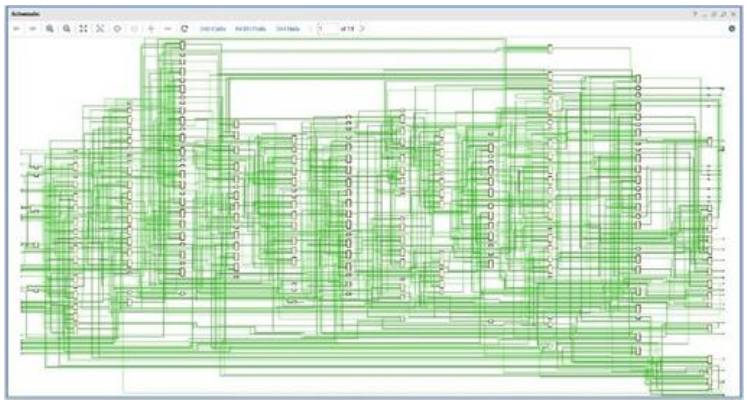

**Fig. 12.** RTL Schematic (Post-Synthesis) View (1)

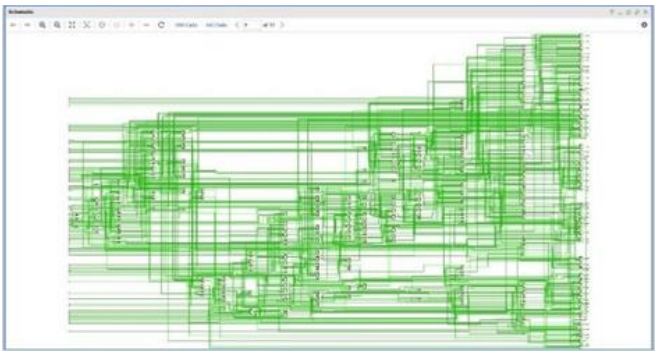

**Fig. 13.** RTL Schematic (Post-Synthesis) View (2)

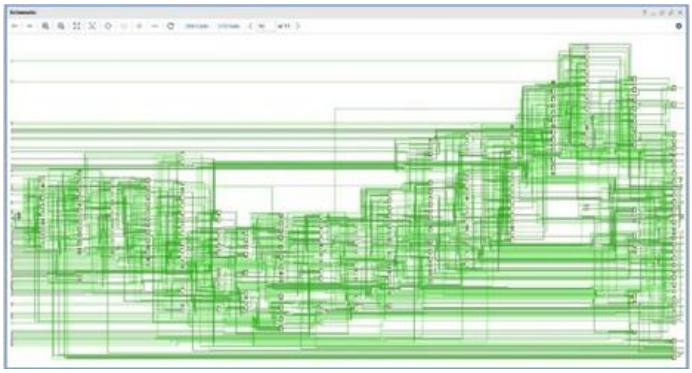

**Fig. 14.** RTL Schematic (Post-Synthesis) View (3)

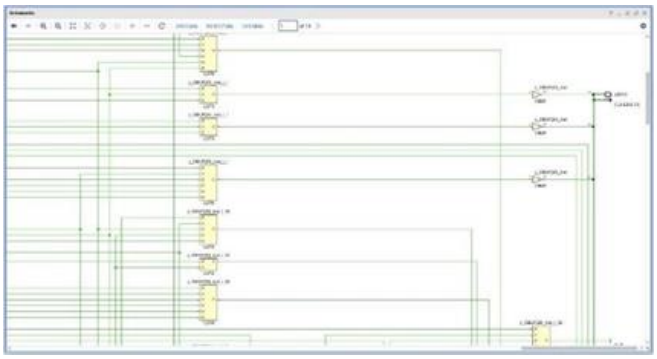

**Fig. 15.** RTL Schematic (Post-Synthesis) View (4)

- Min-Max Combinational Delay Analysis:

The proposed architecture of the multiplier using fundamentals of the vedic mathematics is purely combinational logic circuit. For 32x32 multiplier component, the combinational delay from each of the input buffer to the each of the output buffer is disclosed through the Fig.16 and the Fig.17.

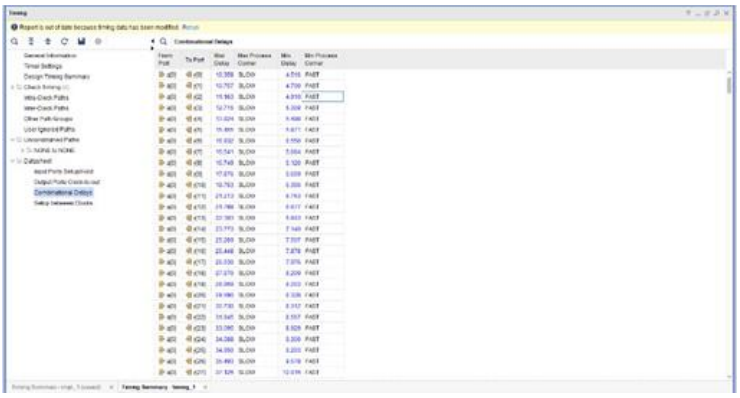

**Fig. 16.** Min-Max Combinational Delay (1)

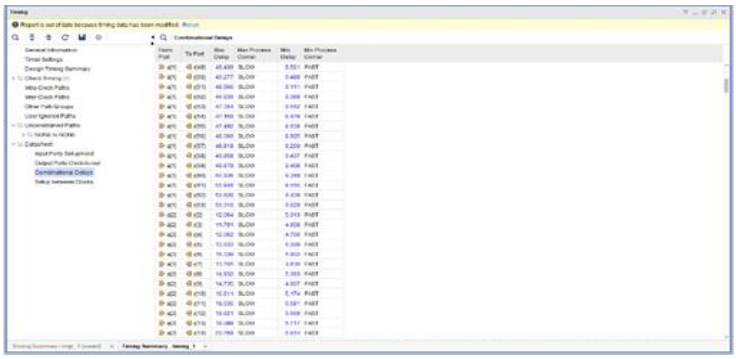

**Fig. 17.** Min-Max Combinational Delay (2)

*C. Statistical Analysis:*

After implementation of the component, described using HDL, HLS can be used for estimation of the different parameters like resources utilized, delay in the circuit and hence the highest frequency and finally the power utilization. Table VI discloses the statistics obtained after implementation of the multiplier component using vedic principles. The analysis is disclosed for different multiplier architecture like 4x4, 8x8, 16x16 and 32x32 multiplier architecture.

**TABLE VI.** STATISTICAL ANALYSIS OF MULTIPLIER ARCHIETCTURE TARGETTING TO XILINX VIRTEX-7 FPGA

| **Multiplier Size** | **Post ImplementationAnalysis** | |
|---|---|---|
| | ***Particulars*** | ***Number*** |
| **4x4 Vedic** | Resources Utilization | 44 |
| | Combinational Delay*(ns)* | Logic: 1.280 |
| | | Route: 0.776<br>Total: 2.057 |
| | Estimated Frequency*(MHz)* | 486.145 |
| | Estimated Power Utilization*(mW)* | Logic: 0.102<br>Route: 4.045<br>Total: 4.147 |
| | Resources Utilization | 189 |

| | | |
|---|---|---|
| **8x8 Vedic Multipli er** | Combinational Delay*(ns)* | Logic: 1.341<br>Route: 0.766<br>Total: 2.107 |
| | Estimated Frequency*(MHz)* | 474.608 |
| | Estimated Power Utilization *(mW)* | Logic: 1.296<br>Route: 12.699<br>Total: 13.995 |
| **16x16 Vedic Multipli er** | Resources Utilization | 763 |
| | Combinational Delay*(ns)* | Logic: 1.283<br>Route: 0.863<br>Total: 2.146 |
| | Estimated Frequency*(MHz)* | 465.983 |
| | Estimated Power Utilization *(mW)* | Logic: 9.699<br>Route: 35.73<br>Total: 45.429 |
| **32x32 Vedic Multipli er** | Resources Utilization | 2940 |
| | Combinational Delay*(ns)* | Logic: 1.285<br>Route: 1.295<br>Total: 2.580 |
| | Estimated Frequency*(MHz)* | 387.597 |
| | Estimated Power Utilization *(mW)* | Logic: 54.562<br>Route: 103.182<br>Total: 157.744 |

After critically analysing the statistics of the multiplier architecture obtained by targeting the description to Xilinx Virtex-7 FPGA device, it is observed that as the complexity of the architecture is increased from 4x4 multiplier to 16x16 multiplier, the delay contributed by routing of the signals is gradually increasing and when the complexity is doubled, the routing delay increases rapidly and becomes more than the logic delay.

## 5. Conclusion

Considering the hardware intensive architecture of the multiplier component, new variant of the multiplication architecture, designed using vedic principles, is described using VHDL and implemented using Xilinx Vivado 2018.2 HLS tool. The design is targeted to the different variants of the FPGA like Vitex, Artix and Kintex series FPGAs. Through this paper the extracted results for Xilinx Virtex-7 General Purpose Series FPGA are disclosed. Through various verification steps like simulation, synthesis and implementation the proposed architecture is verified and statistical analysis is carried out by extracting the results with respect to the resource utilization, delay contributed by different component and routing and hence estimated maximum frequency of operation and maximum power utilization.

After going through the statistics in Table VI, it is observed that the resources utilized, as expected, are increasing according to the complexity. Since the complexity is increasing the delay contributed is increasing and hence, the estimated frequency is decreasing through the increment of the complexity. The power dissipation is also increasing according to the complexity. When the analysis is carried out for delay parameter, it is observed that the delay is gradually increasing when the complexity is increased from 4x4 multiplier to 16x16 multiplier architecture, but it increases

further rapidly when the complexity is doubled. Further, after splitting the total delay into logic delay and routing delay, it is observed that after complexity of the 16x16 multiplier architecture, due to increase in the complexity, the routing delay becomes more than that of the logic delay, as depicted in the Fig.18.

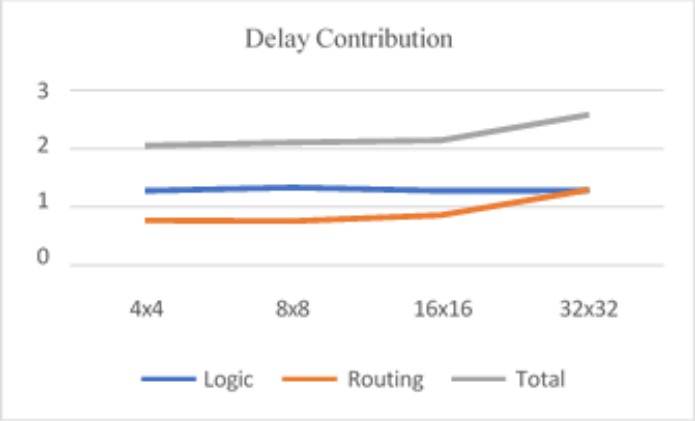


**Fig. 18.** Delay Contribution

It means that after increasing the delay upon certain limit, the amount of delay contributed by routing becomes more as compared to the logic delay. In other words, the time required to process the data becomes less than that of the handling the data. This becomes the drawback of the architecture. To address this issue, it is possible to reconstruct the same architecture using modern sophisticated tools like Cadence. In Cadence tool it is possible to design Application Specific Integrated Circuit variant of the HDL description where low routing delay is expected.

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