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Ultra Efficient Reversible Logic Multiplier Design and Implementation for Low Power Application

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Abstract: In recent years reversible logic has appeared as one of the most encouraging research fields. It has found application in a variety of technologies including low-power CMOS, nano-computing and optical computing etc. It is well known that reversible logic work with future computing technologies that almost emit less heat with negligible power dissipation. This research paper gives the in-depth comparative analysis and design of the different circuits that can be for DSP processor design for low power application using the reversible logic. Paper basically focused on the modified transistorized design and implementation of basic gate like Toffoli Gate, proposed gate like HAG,FAG, FAG1, Half adder and Full adder design, 2*2 multiplier, 4*4 multiplier design and its comparison for the different parameter such as number of transistor required, Gate count, Power Dissipation. In comparative analysis of 4*4 multiplier average power dissipation is found to be 120uW that gives enormous amount of power reduction in the proposed design as compared to existing design available. Design and simulation is done using Tanner EDA tool V13 with 180nm technology file.

Keywords: *Reversible Logic, Low power, Adder, Multiplier design, Ancilla bits, Garbage outputs*

1. Introduction

For irreversible logic calculations researchers like Landauer have demonstrated that each bit of data erase results K.T.ln(2)Joules heat energy, where K is the Boltzmann constant and T is the temperature [1]. Since the amount of energy dissipated in a system directly correlates to the number of bits lost during calculation, Bennett demonstrated that K.T.ln2 energy dissipation would not occur if a computation is carried out in a reversible method[2]. Circuits that retain input information called reversible circuits. Only reversible gates allow for the performance of reversible computing in a system. These circuits have a one to one correspondence between input and output vectors, meaning that each input vector can produce a distinct output vector and vice versa. Consequently an NXN reversible gate can be described as

IN=(I1,I2,I3,I4,……IN)

ON=(O1,O2,O3,…….ON).

Multiplication is one of the crucial arithmetic operations in many applications such as signal processing and communication. The fundamental limitations of the multiplication operation, which is involved in signal processing, are latency and precision. Reduction in the number of computation is required to increase the speed of the multiplier circuit. Multiplier is basic building block for any Arithmetic and logical unit design. In this paper we proposed the design of new reversible gate and its application as a multiplier for 2*2 and 4*4 bit multiplication. There are two important stages in the multiplier design one is partial product generation and second is the addition sub circuit. Paper is arranged in such a way section 2 give brief about literature of review. Section 3 & 4 describe the proposed gate and application with its functionality. Section 5 gives the result and comparison of proposed multiplier with the existing one.

2. Literature Survey

S. Sharmila Devi, V. Bhanumathi [3] proposed MCML (MOS Current Mode Logic) based reversible full adder in term of improved speed and reduced power dissipation when it related with CMOS logic. A suggested circuit performs better than existing reversible logic circuits for the different parameters. Hari Mohan Gaur et.al.[4] presented a comparative analysis of Reversible Gates to obtained best design in the circuits. RC-viewer tool used for implementation. The evaluation is carried out at two further levels namely the circuit design level and the gates structural level and it offers a superior method for building logic circuits. This paper [5] author proposed reversible KMD Gates to find different factors like fault tolerance, fault coverage and fault detection. Also showed quantum equivalent and controlled V and V+ gate in all the types of KMD Gates and showed that significant reduction in quantum cost. Author implemented [6] Mux and Demux circuits and simulated on Vivado (v2016.4). The proposed

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circuits give better results in terms of energy and Gate count. Research paper [7] described URG reversible gate that can be used to build a reversible FPGA and replicate the capabilities of a lookup table (LUT). Design online testable circuit that is capable of spotting any single-bit faults. In this Paper [8] author proposed BCD adder using RLG gate and GDI logic. Oleg Golubitsky and Dmitri Maslov [9] present two algorithms to synthesize an optimal circuit for any 4 bit reversible specification. PFAG and HNG are used to implement the reversible ripple carry adders. Reversible logic can be used to enhance the performance of ripple carry adder circuits. Evaluations of the number of gates used, trash output, quantum cost, and delay of ripple carry adders implemented with reversible logic gates revealed a 2.01 energy saving ratio [10]. Author [11] proposed new design method for Decimal to BCD encoder using reversible logic through PG and FG gate. The proper placement of the gates has allowed for the decrease of GC (gate count), QC (quantum cost) and GO garbage outputs). This paper [12] proposed the novel designs of latches and flip flops using FG and FRD and TG gate. For optimization two novel reversible gates the modified Fredkin gate (MFG) and the Toffoli gate (MTG) are also presented along with its transistor design used for reversible sequential circuits. Paper [13] proposed new full/half adder reversible design by combining the CNOT, CCNOT, and CSWAP gates. The proposed reversible full/half adder is effective in lowering the number of transistors, gates, and constant inputs (ancilla bits). In comparison to previous work already published in the literature, the suggested complete adder demonstrates a 47% decrease in power dissipation, a 33% reduction in constant inputs, a 50% reduction in garbage outputs, and a 67% reduction in transistor count. Author presented [15] a new design approach for 4-bit multiplier array circuit using WG and BME gate with reversible approach. Author [16] focused on the design of reversible multipliers and showed two solutions that reduced quantum cost in comparison to similar designs. They also included an adder circuit to the multiplier, which improved resource utilization. PG and TG is used for partial product generation in design I, II. It is described how an adder circuit and multiplier were integrated into the design to make advantage of the multipliers' unused capacity. Comparing the proposed circuit reversible logic multiplier to existing designs, it has lesser hardware complexity in terms of quantum cost. Research paper proposed a novel 4×4 bit reversible multiplier circuit. The reversible multiplier circuit is built using MKG, HNG gates. The two 4-bit binary numbers can be multiplied by the suggested reversible multiplier circuit. Study, signed Baugh-Wooley multiplier circuits using reversible gates and an unsigned four-bit array multiplier are developed [17-20].

3. Design and Implementation Proposed Reversible Basic Gates

3.1. Modified Transistor Implementation design of Toffoli Gate

Toffoli gate is 3 input (A,B,C) & 3 output (P,Q,R) gate where output P and Q are same as input A and B and Q is equal to (AB XOR C) as shown in Fig.1. In Proposed gate number of Transistors required less for performing the operation.Fig. 2 waveform represent the simulation result for TG and it can be verified according to truth table for output R. Power dissipation is 11.988uW which is less power dissipation as compare to the result available in the literature.

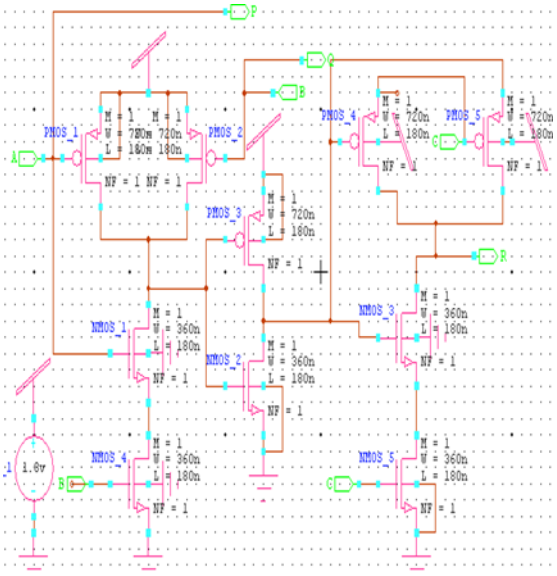

Fig.1 Transistor Implementation of modified Toffoli Gate

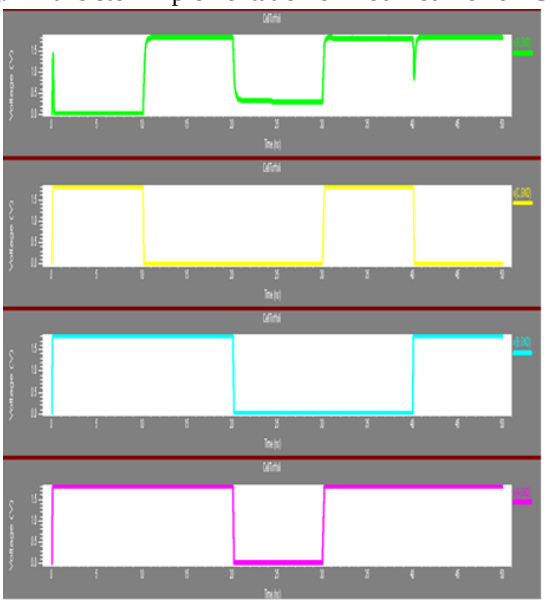

Fig.2 Waveform for Proposed Toffoli Gate (TG)

3.2Proposed FAG1 Gate Transistorized Design:

Proposed design can compared with the existing TSG gate. It is having 3*3 inputs and outputs which single gate will

work as a Full Adder. Input bits are applied to the (A,B,C) and output is generated at (P,Q,R). Output P= A XOR B, Q= Sum and R= Carry. Number of transistor required for the implementation is 16. Power requirement is 3.2400*10-12W which is very small when compared with the Full Adder using TSG. Figure bellow shows the simulation result for proposed FAG1 gate.

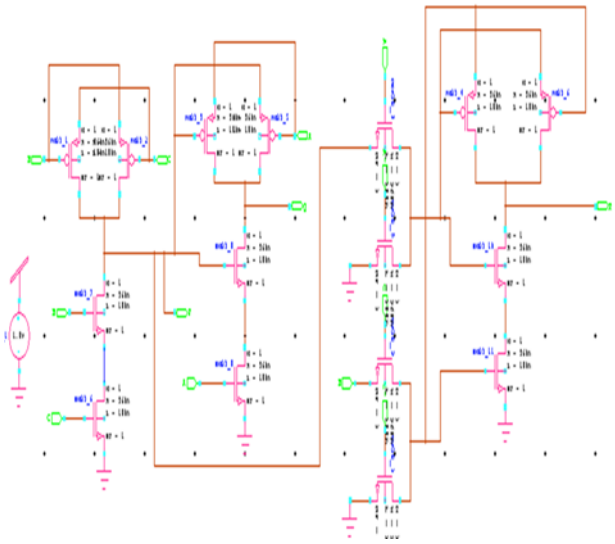

Fig. 3 Transistor Implementation Modified FAG1 Gate

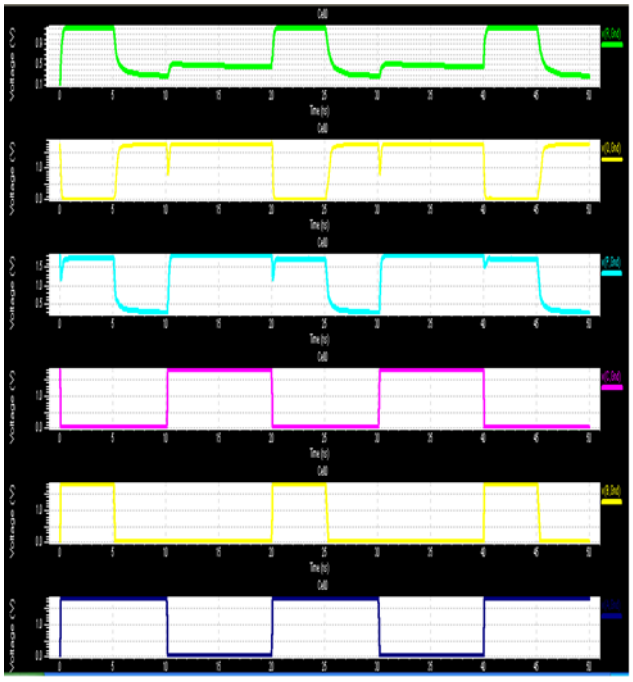

Fig.4 Simulation Waveform for modified FAG1 Gate

3.3. Proposed New HAG gate

Fig.5. HAG Gate

Table1. Truth table for HAG Gate

Input		Output	
A	B	P	R
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

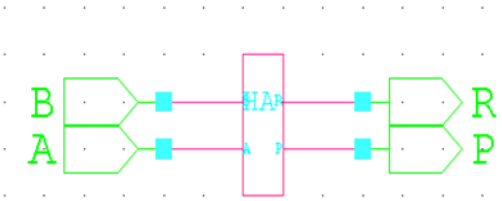

Fig6. Symbol representation of HAG

3.4 ProposedTransistorized Iimplementation of HAG

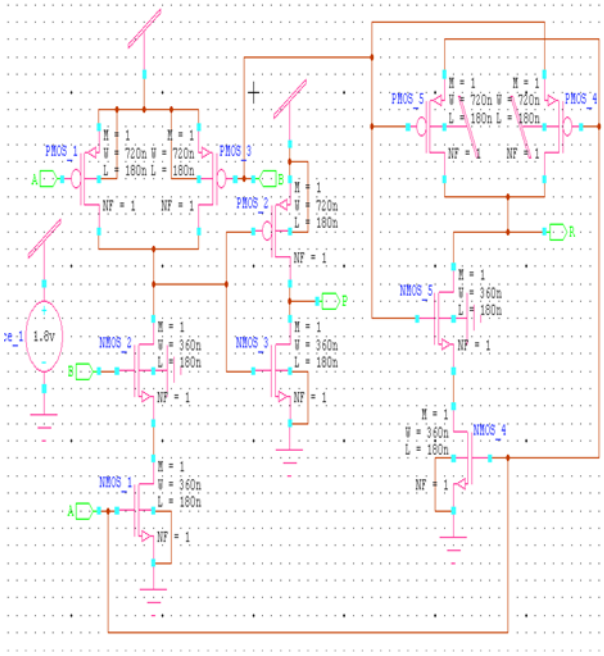

Fig. 7 Transistorized implementation of HAG

Proposed HAG gate work as a Half Adder. It is having two inputs (A & B) and two outputs (P & Q). Output P is performing AND operation and output Q perform XOR operation. Transistor implementation of Half adder is shown in Fig. 7.

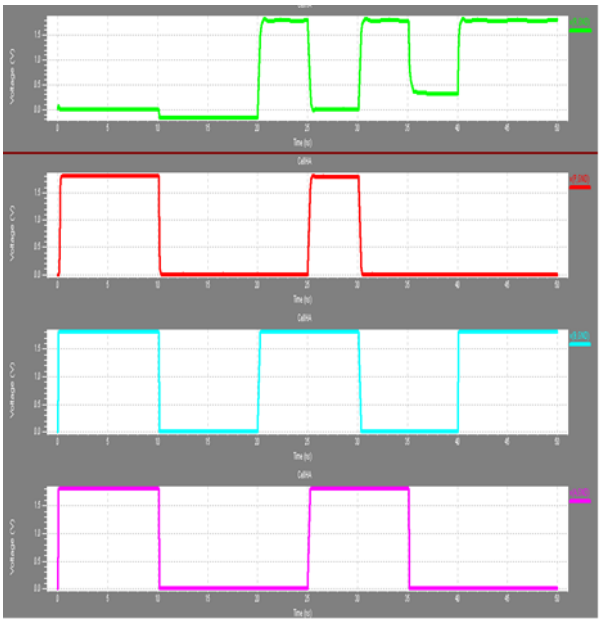

Fig. 8 Output Waveform for Half adder

The simulation result for Half adder using HAG gate shown in Fig. 8 and we can verify it by truth table of HAG gate.

3.5 Proposed FAG gate

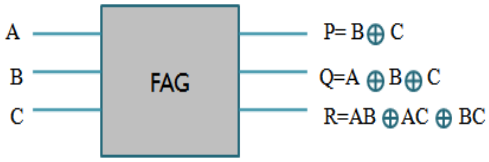

Fig.9. FAG Gate

Table 2: Truth table for FAG Gate

Input			Output		
A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	1	1	0
0	1	0	1	1	0
0	1	1	0	0	1
1	0	0	0	1	0
1	0	1	1	0	1
1	1	0	1	0	1
1	1	1	0	1	1

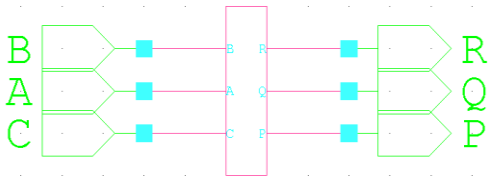

Fig.10 Symbol representation of FAG

3.6. Proposed transistorized implementation of FAG

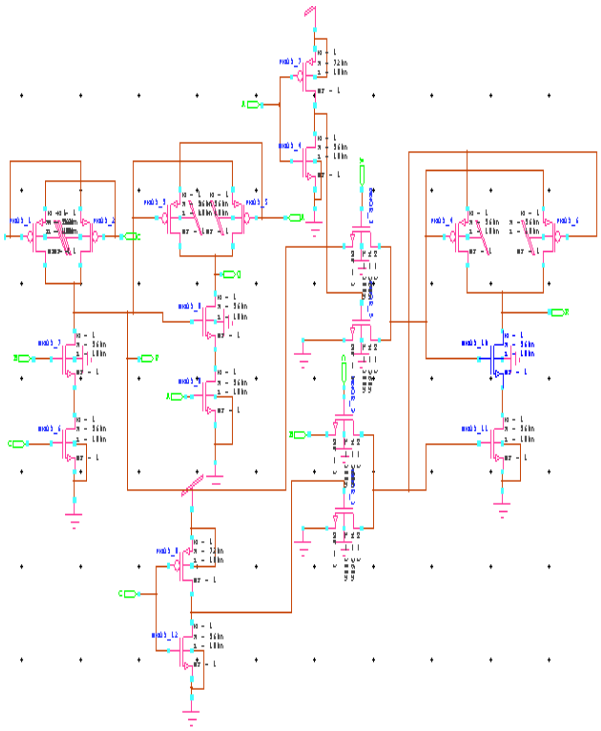

Fig.11 Transistorized implementation of FAG

FAG is 3*3 gate perform Full adder operation. It is having 3 input (A, B, C) and 3 output (P,Q,R). Output P perform XOR operation of input bit B and C. Output Q perform Sum operation and output R gives Carry operation for full adder. Symbol creation is shown in fig. 10. Transistorized implementation of FAG gate is shown in fig 11. Total 20 transistors required for construction.

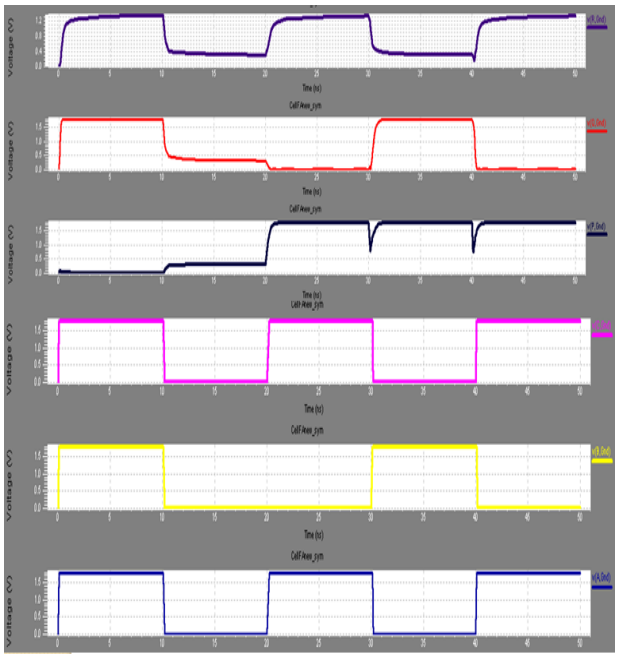

Fig.12 Simulation Waveform for FAG

The simulation waveform shown in Fig.12 for FAG Gate and it can be verified by its truth table. This FAG gate is used for the construction of arithmetic sub circuit in 4*4 multiplier design.

4. Application of Proposed gate HAG and FAG for 2*2 and 4*4 Multiplier Design.

4.1 Proposed 2*2 Multiplier

Multiplier is essential functional unit in most of the processors and multiplication is one of the important arithmetic operations.

		Y1	Y0
		X1	X0
+		Y1X0	Y0X0
	Y1X1	Y0X1	
S3	S2	S1	S0

In 2*2 multiplication process proposed HAG gate are used for Partial product generation as well as arithmetic sub circuit. Total 6 HAG gates are required for 2*2 multiplier design. The actual design is shown in Fig. 13.

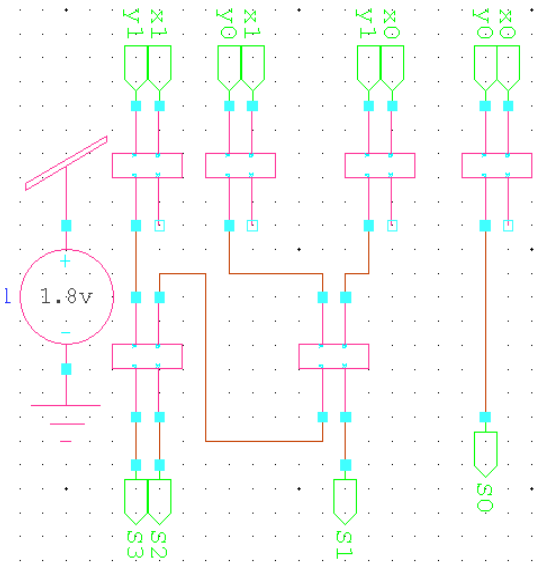

Fig.13 Design of 2*2 Multiplier using the Proposed HAG gate

Partial product terms are generated using AND operation of HAG gate and for generation of addition sub circuit i.e. P0, P1, P2, P3 XOR operations of HAG gates is used.

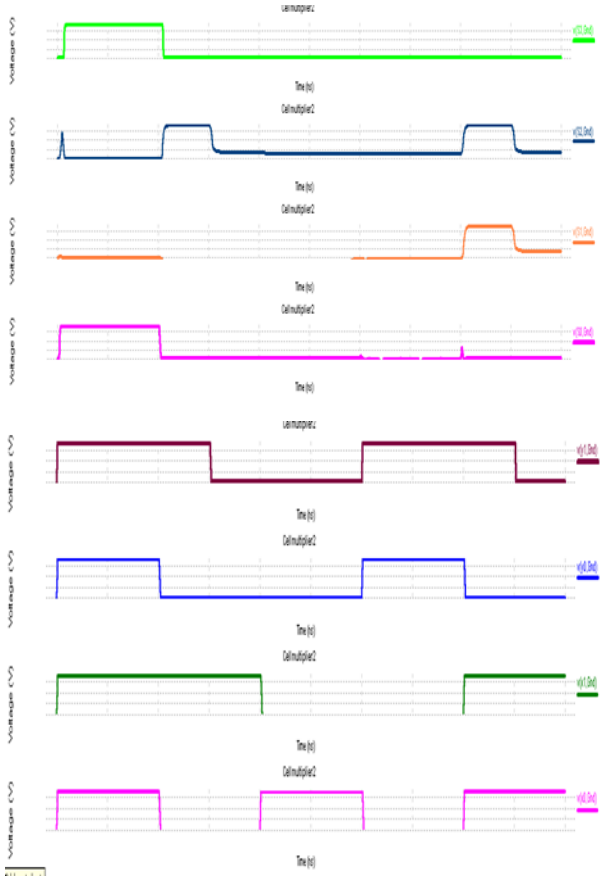

Fig. 14 Simulation waveform of 2*2 Multiplier

Consider the Input bits (Y1, Y0 and X1, X0) is (1,1 and 1,1) respectively output is 1001 which can be verified from the simulation results shown in Fig 14. Measurement result summary after simulation shows the average power =16.8uW.

4.2Proposed Design of 4*4 Multiplier

4.2.1Partial product (PP) generation

			y3	y2	y1	y0	
		*	x3	x2	x1	x0	
			xoy3	xoy2	xoy1	x0y0	PP1
		x1y3	x1y2	x1y1	x1y0		PP2
+	x2y3	x2y2	x2y1	x2y0			PP3
x3y3	x3y2	x3y1	x3y0				PP4
s7	s5	s4	s3	s2	s1	s0	

For the design of N*N multipliers partial products require n*n AND operations with two inputs. In order to build the partial products i.e. PP1, PP2, PP3, PP4 depicted in above we used proposed HAG gate which is acting as a Half

adder. Addition of all the PP terms is performed using CSA. In carry save adder method the two bit addition done by half adders using HAG gate. Using CSA large number of addition can be performing very quickly. For the generation of summing output of S2 to S7 combination of HAG and FAG gates are used. The carry generated during the operation diagonally transfer to the next column of the addition sub-circuit. 4*4 multiplier consists of 16 AND operation using HAG gate, eight full adder logic circuits using FAG gate, and four half adder logic circuits using HAG gate. The final design of 4*4 multiplier is shown in figure 15.

				0	1	0	1	→	5
			*	0	0	1	1	→	3
				0	1	0	1		
			+	0	1	0	1		
		0	0	0	0				
	0	0	0	0					
0	0	0	0	1	1	1	1	→	15
S7	S6	S5	S4	S3	S2	S1	S0		

Results can be verified for the input bit pattern Y3=0, Y2=1,Y1=0,Y0=1 and X3=0, X2=0, X1=1, X0=1. And from the output waveform shown in Fig 16. it can be verified. The Power dissipation for the proposed multiplier is 126.10uW which will show the drastic improvement in in power dissipation as compare to existing paper [19].

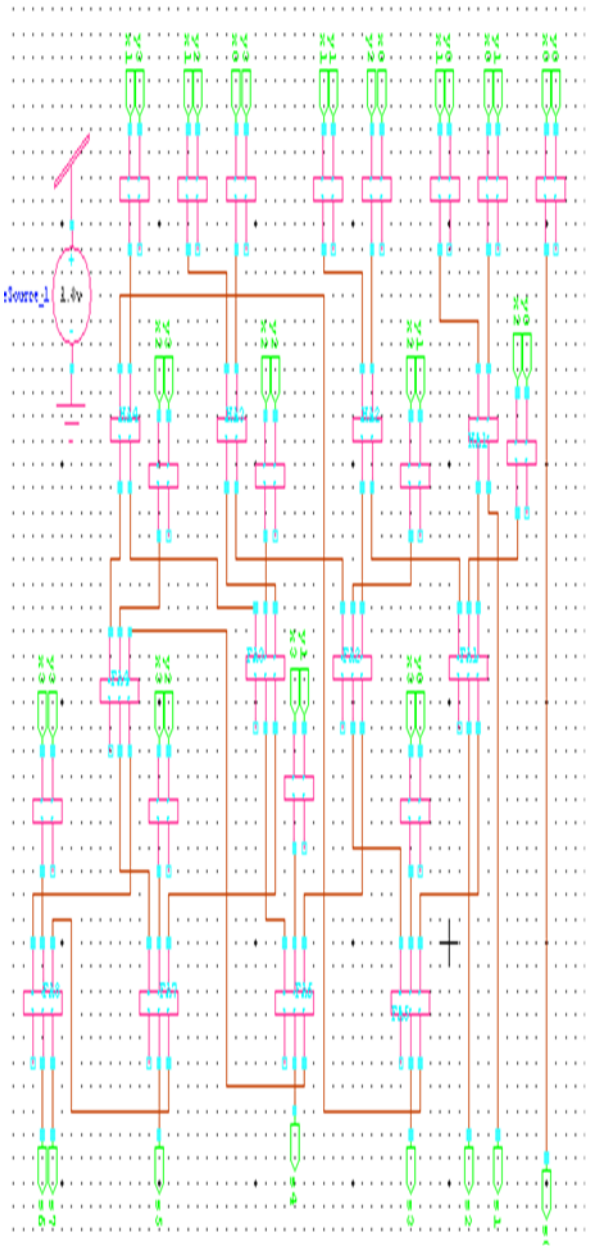

Fig.15 Design of 4*4 Multiplier using the proposed gate

5. Result and Discussion

The comparative power analysis has been done for the different reversible gate as showed in table 3 and proposed gate shows the improvement in power dissipation.Proposed Full adder circuits compared with the existing design compared for the different parameter. Proposed Power efficient 4*4 bit array multiplier analyzed for the different parameter likes total gates, transistor required, ancilla input, garbage output, power dissipation etc. for the signal transition from 1ns to 50ns. Proposed reversible design for 4*4 multiplier has great improvement for different parameter.

Table 3. Comparative Result for Proposed Gate

Sr. No.	*Particulars*	No. of transistor Required	Power Dissipation
1.	Toffoli Gate (Proposed)	10	11.988uW
2.	Toffoli Gate (Existing)	12	15.096uW
3.	Proposed Transistorized design FAG1	16	$3.2400*10^{-12}$ W
4.	Full Adder using TSG (Existing)	22	$6.0702*10^{-8}$ W

Table 3 shows comparison the number of transistor Required, power dissipation for Toffoli gate and TSG Gate which are available in Literature with proposed design.

Table 4. Comparative Result for Full adder

Adder	Total Gates	Total Transistors	Ancilla Inputs	Garbage Outputs	Power Dissipation (μW)
Proposed Full Adder FAG	1	20	0	1	2.1097 uW
Full adder Existing [10]	4	48	2	2	13.3 uW
Full adder Existing [13]	2	-	1	2	-

Table 4 shows the performance comparison of different full adder architecture and proposed design there is a remarkable improvement in parameter like total gates, and total transistor required, Ancilla Input, Garbage output and Power dissipation

Table 5: Performance Comparison of Different Multiplier Architecture

Multiplier	Gates Required	Total Gate	Ancila Input or Constant Input	Garbage Outputs (GO)	Average Power Dissipation (μW)	Delay (nS)
Proposed Multiplier	**HAG FAG**	**28**	**0**	**24**	**126.10 uW**	**9.9143 nS**
Existing Multiplier Design [16]	Design I	32	36	28	-	-
	Design II	*28*	*28*	24	-	-
Existing Multiplier Design [15]	*BME, WG*	*20*	-	25	-	-
Existing Multiplier Design [18]	*MKG and PG*	*28*	-	56	-	-
Existing Multiplier Design [19]	*RSG, DPG*	*20*	-	28	28.7 mW	16.322 nS

Table 5 shows the comparison of 4*4 multiplier available in literature in terms of the gate count, constant input, garbage output, average power dissipation. Proposed multiplier required 28 total gates, constant input is 0 garbage output is 24 and most important the very less power dissipation as compare to the existing paper [19]

6. Conclusion

Thus we designed and simulated a 4*4 reversible multiplier array using HAG and FAG proposed gate. The proposed designs are compared with the reported one design. The proposed 4*4 bit multiplier is 99% improvement in power dissipations compared to the existing multiplier [19] design using RSG and DPG gate. In proposed design 14.28% improvement in garbage output. There is no requirement of constant input in proposed implementation. The proposed design of 4*4 reversible multiplier circuit is advantageous for low power, high speed computing applications like in case of DSP processor, optical communication etc.

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