International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

'Power-Aware-Test: Methodology for Test Power Analysis and Reduction'

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Submitted: 09/12/2023 **Revised**: 18/01/2024 **Accepted**: 28/01/2024

Abstract: Facilitating testability in design is pivotal in the integrated circuit design cycle, incorporating logic to facilitate comprehensive defect testing during manufacturing. However, this addition introduces challenges, particularly regarding power requirements during testing. The consideration of power aspects in the design cycle is crucial, as instances exist where chip failures attributed to power issues during testing have adversely impacted overall yield. Balancing the imperative for thorough testing with the potential power-related pitfalls is integral to ensuring the reliability and success of the integrated circuit in the manufacturing process.

Key words: *1. Power-Aware-Test, Semiconductor testing, Design-for-Testability (DFT), Multibit mapping, ATPG (Automatic Test Pattern Generation), Scan architecture, Dynamic power, Multibit reordering, Q-gating, Test power reduction, EDA (Electronic Design Automation)*

1. Introduction

The landscape of semiconductor testing is undergoing a transformative shift, as the industry increasingly recognizes the imperative of energy efficiency. This shift has led to the emergence of innovative methodologies, with a particular focus on addressing the challenges associated with power consumption during the testing phase. The concept of "Power-Aware-Test" has evolved as a distinct research domain, underscoring the necessity for a comprehensive approach to power analysis and reduction in semiconductor testing. Traditional testing practices, while effective in ensuring the functionality of integrated circuits (ICs), often result in significant power wastage. This not only raises environmental concerns but also contributes to escalating operational costs. This paper aims to delve into the nuanced facets of Power-Aware-Test, exploring its methodologies, implications, and contributions to the broader goals of sustainable technology development.

Semiconductor testing has traditionally emphasized functionality and reliability, often neglecting the critical aspect of power consumption. Wang et al. (2017) point out that power consumed during testing can constitute a substantial portion of the overall power budget of an integrated circuit. To address this challenge, the Power-Aware-Test paradigm seeks to reconcile the tension between accurate testing and minimal power consumption. This paradigm shift aligns with the global push towards energy efficiency and environmental responsibility. The growing realization that traditional testing practices may not align with these broader goals has prompted a reevaluation of testing methodologies.

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The increasing complexity of modern integrated circuits, coupled with the prevalence of portable electronic devices, accentuates the need for efficient power-aware testing methodologies. Zhang et al. (2018) argue that the conventional one-size-fits-all testing strategy, often applied to all components of an integrated circuit, neglects the inherent variations in power consumption across different modules. This lack of granularity in testing methodologies can lead to significant power overheads. In response, the Power-Aware-Test paradigm seeks to tailor testing strategies to the specific power characteristics of individual components. This approach resonates with the broader trend towards precision testing and optimization, as highlighted by Li et al. (2016), where targeted power reduction efforts can be more effectively deployed.

Power-Aware-Test not only addresses power consumption during testing but also incorporates a proactive analysis of power profiles to optimize test strategies. Kim et al. (2019) emphasize the importance of comprehensive power analysis tools to understand the dynamic power behavior of integrated circuits during the testing process. Integrating these tools into the testing methodology allows researchers to gain valuable insights into power-hungry regions and devise targeted strategies to reduce power consumption without compromising on test quality. This proactive stance aligns with the broader industry trend of incorporating design-for-testability (DFT) principles into semiconductor testing, ensuring that power considerations are embedded in the design and testing phases.

Furthermore, the Power-Aware-Test paradigm contributes significantly to the broader landscape of

sustainable technology development. In a world increasingly focused on environmental sustainability, the semiconductor industry faces mounting pressure to reduce its carbon footprint. Wang et al. (2018) emphasize that addressing power consumption in testing is a crucial step toward achieving this goal. By adopting power-aware testing methodologies, the industry can not only meet regulatory requirements but also enhance its reputation as a responsible contributor to technological advancement. This alignment with broader environmental goals positions Power-Aware-Test as a critical area of research with far-reaching implications for the future of semiconductor technology.

The implications of Power-Aware-Test extend beyond the technical realm into the broader societal and environmental context. As semiconductor technology continues to permeate every aspect of modern life, its environmental impact becomes a growing concern. The traditional view of technological progress often omits the hidden costs associated with power consumption during testing. The Power-Aware-Test paradigm, with its emphasis on minimizing power consumption without compromising on testing accuracy, aligns with the broader societal shift towards sustainable practices.

2. Description of Work Done

The objective of this investigation is to incorporate technologies for reducing test power in a propose, evaluate test power using the test power method [8], and compare the results with a baseline flow that lacks test authority reduction methods.

Baseline run Details-

The design comprises 500K instances, employing a 22nm technology library.

The established flow remains as follows.

Baseline run:

1. Execute design synthesis.
2. Integrate Design for Testability (DFT).
3. Conduct Automatic Test Pattern Generation (ATPG) at 40 kHz.
4. Simulate test models and generate shifting activity files.
5. Quantify test power.

Test Power Reduction run-

1. Conduct proposal synthesis.

   Apply Multibit mapping.

   Implement Multibit reordering.
2. Integrate Design for Testability (DFT).

   Utilize Q-Gating.
3. Execute Automatic Test Pattern Generation (ATPG) at both 20 kHz and 40 kHz.
4. Simulate the generated test configurations and produce switching doings files.
5. Evaluate and compare Test power with the Baseline run.

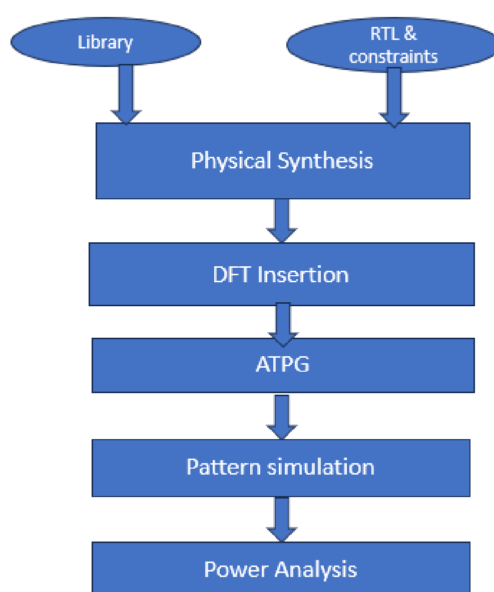

Fig 1: Baseline design flow

Step1: Conduct physical synthesis with multibit registers. Following the initial synthesis pass, integrate DFT logic using the Synopsys DFT compiler tool. Employ the typical DFT insertion flow as described below.

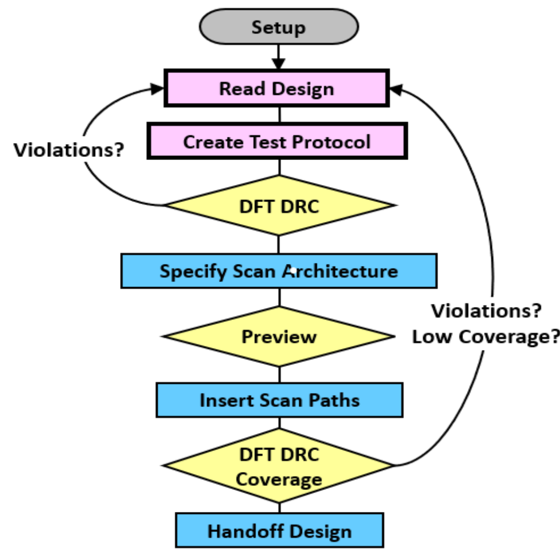

Fig 2 DFT insertion flow

Post DFT logic insertion, the Synthesis tool executes an additional round of incremental optimization to restore the quality of results.

The scan planning consists of 8 top-level examination chains and 96 interior scan chains, configured with scan density as specified below.

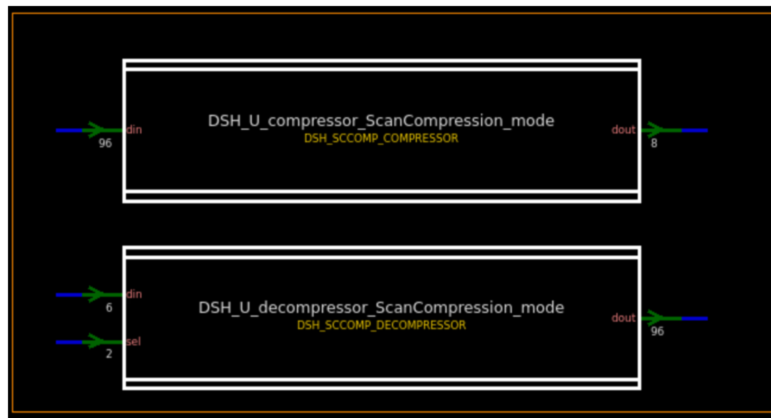

Fig 3: Scan Configuration

Step2: Following DFT insertion, the design is transferred to the ATPG tool for generating patterns. The objective is Evolution Interruption Fault outline generation, and a standard TDF pattern is illustrated below.

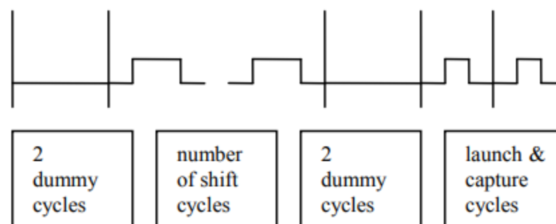

Fig 3: A Typical TDF pattern.

Step3: Simulate chosen patterns with the Synopsys VCS tool, generating an FSDB (switching activity file) to record net transitions.

Step4: Utilizing the switches file (FSDB), perform power assessment and scrutiny with the EDA tool, Synopsys PTPX.

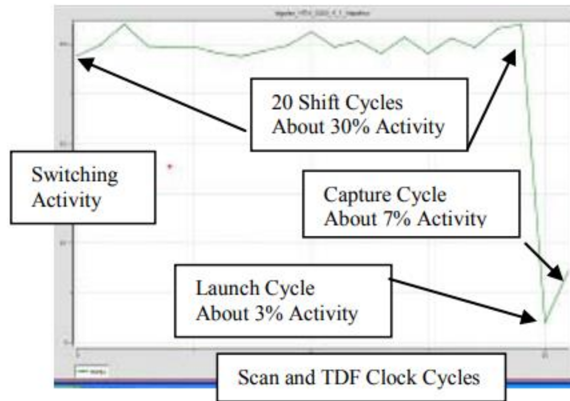

Fig 4: Switching activity of TDF pattern.

Observations reveal a 30% switching motion during scan changing, attributed to the activation of all fall down in the design. Additionally, during start on, there is 3% activity, and during gain control, at the functional frequency, the activity increases to 7%.

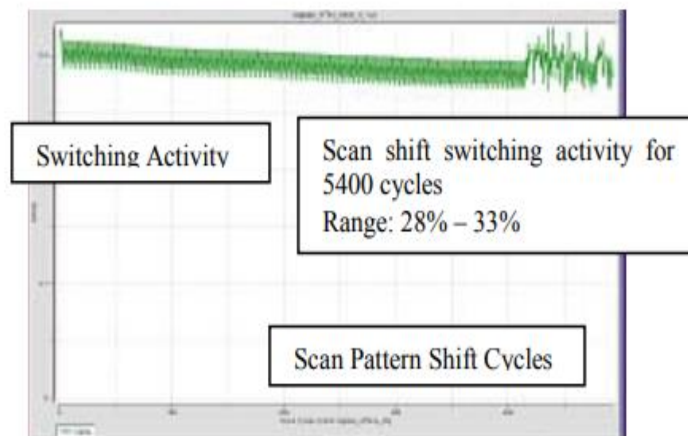

Fig 5: Switching activity of entire scan pattern.

TDF Pattern	Average Power (mW)	Dynamic Power (mW)	Static Power (mW)
1st	818	668	150
2nd	833	683	150
3rd	856	706	150
4th	860	710	150
5th	863	713	150

Table1: Power estimation results for TDF patterns

Attributes

u - User defined power group
i - Includes clock pin internal power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00
clock_network	1.97e+04	5.60e+04	2.05e+00	7.57e+04
register	2.17e+03	2.98e+02	1.66e+02	2.63e+03
sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00
combinational	3.36e+03	5.38e+03	4.81e+02	9.22e+03
Total	2.52e+04 uW	6.17e+04 uW	6.49e+02 uW	8.75e+04 uW

Table2: Functional power estimation for baseline run.

The dynamic power is higher than anticipated, primarily influenced by the switching activity during scan shifting. Conversely, static power remains consistent across the technology node, aligning with expectations.

3. **Test Power Reduction Flow Details**:

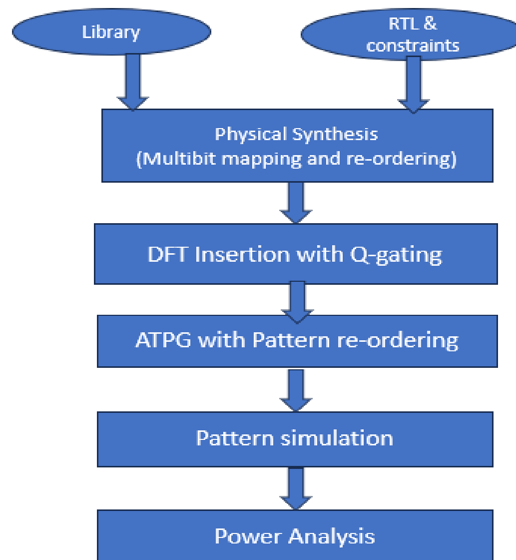

Fig 6: 'Test Power reduction flow'

The aim of this process is to minimize test operate, and to achieve this:

1. During manufacture, records are aligned with multibit library cells.
2. Reordering of bits is implemented in a multibit configuration.

a. Comprehensive consideration is given to combinational switching.

b. Connecting the least active bit to the scan-out of the multibit cell is executed as follows.

c. Prior to reordering, the A [3] bit contributed to a substantial combinational logic cloud, while the A[2] bit influenced a smaller cloud.

d. Following the reordering process, the connection of the A[2] bit to the scan-out results in reduced switching during scan shifting, consequently lowering dynamic power.

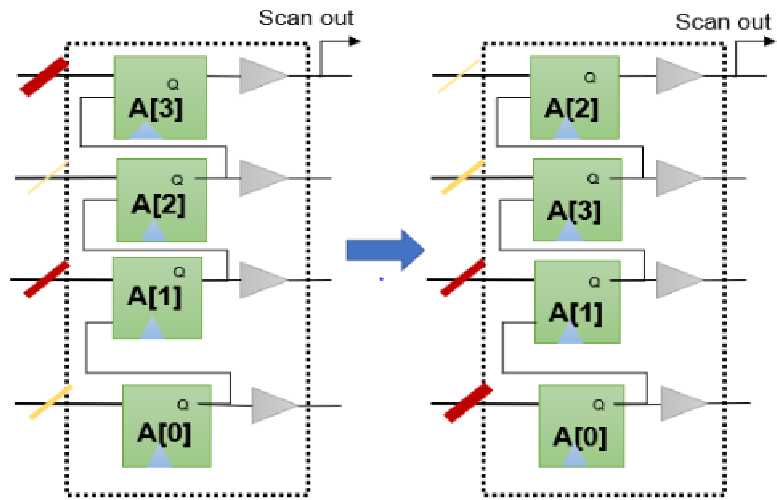

Fig 7: ‘Multibit cell before and after bit re-ordering’

Q-gating is an additional method wherein the Q of the transmission is gated using scan regulate indications, effectively suppressing combinable logic switching during scan changing.

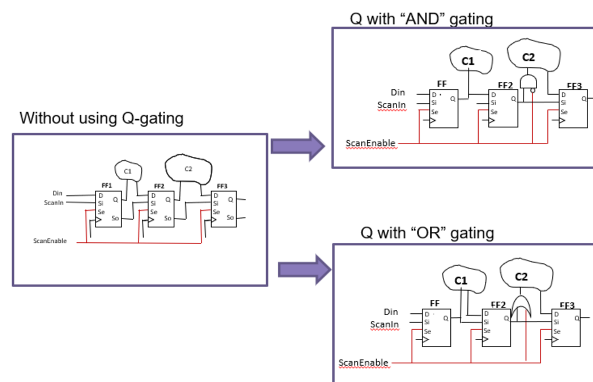

Fig 8: ‘Q-Gating technique’

ATPG patterns are generated to minimize switching activity during transitions between different design patterns. The power evaluation for the test power decrease flow is outlined as follows.

TDF Pattern	Average Power (mW)	Dynamic Power (mW)	Static Power (mW)
First	663	513	150
Second	626	476	150
Third	613	463	150
Fourth	645	495	150
Fifth	628	478	150

Table3: Power inference results for TDF pattern for test power decrease issue

Attributes

u - User defined power group
i - Includes clock pin internal power

Power Group	Internal Power	Switching Power	Leakage Power	Total Power
io_pad	0.00e+00	0.00e+00	0.00e+00	0.00e+00
memory	0.00e+00	0.00e+00	0.00e+00	0.00e+00
black_box	0.00e+00	0.00e+00	0.00e+00	0.00e+00
clock_network	1.97e+04	5.58e+04	2.04e+00	7.55e+04
register	2.15e+03	3.45e+02	1.66e+02	2.66e+03
sequential	0.00e+00	0.00e+00	0.00e+00	0.00e+00
combinational	3.30e+03	5.14e+03	5.09e+02	8.95e+03
Total	2.52e+04 uW	6.13e+04 uW	6.77e+02 uW	8.71e+04 uW

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Table 4: 'Functional power estimation for test power reduction run'

4. Inference:

- Elevated transferring activity during scan changing contributes to heightened dynamical energy consumption.
- The adoption of multibit banking proves advantageous, concurrently curbing both functional and test power.
- Multibit re-ordering is instrumental in mitigating combinational switching, achieved by connecting the least active bit to the scan-out.
- The strategic use of Q-gating further diminishes excessive combinable logic switching through examine shifting, effectively cutting dynamical power dissipation.
- The amalgamation of these test power reduction techniques yields a comprehensive solution within the EDA framework, culminating in a substantial reduction in overall test power.

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