International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Low Power and High throughput Reconfigurable FIR Filter Architecture using RRNS for SDR Applications

[1]Dr. Manjunath P. S., [2]Sapna Kumari C., [3]Dr. Rajashekhar U., [4]Dr. Thirthe Gowda M. T., [5]Sharath S.

Submitted: 29/12/2023 **Revised**: 05/02/2024 **Accepted**: 13/02/2024

Abstract: A RNS significant RNS (Residue Number System) FIR filter design forSoftware Defined Radio (SDR) filtration is proposed, with the properties to satisfy such as clustering and concurrency process, this system provides a remarkable performance for the FIR filters. The proposed method is a novel technique for the minimization of the various time delaying parameters with the operation of the Distribution Arithmetic (DA) based residue processing. The proposed FIR filter with core optimized RNS has the benefit of rising performance, lowering processing latency delay with the suitable utilization of the existing RAM blocks on the FPGA, with the simulation results it can be observed that filter size with its operation are channelized and corresponding decrease in the operation logic with FPGA which can be considered as the cost effective as well. One of the major advantage of the proposed system as it can be noted that performance is improved comparatively, the operations which are to be done by the similar experimental setup requires more than 8 taps and 64 tap requires higher order hardware's. The cost effective and high throughput Finite Impulse Response (FIR) Filter is proposed using Reconfigurable Residue Number System (RRNS). The new design proposed here the same benefits as that of, add and shift method used before. The complexity of the system is reduced whenever the RRNS system has been added. The Vivado Design Suite & Artix-7 are used to implement the logical structure created. Inducer complete exercise 64-Tap filter is designed. The binary added is used to replace the classical modulo added. This will enhance the accuracy produced by single modulo reduction stage. The area is reduced by approximately 18%. In comparison with the multiplier in each tap with two's complement filter, the index based arithmetic multifaceted filter diminishes the Quadratic RNS off about a 69%. The newly designed filter requires only 45% of LE when compared to the traditional design.

Keywords: *Reconfigurable FIR filter, Redundant-RNS, Parallel Prefix Adder, QRNS, FPGA*

1. Introduction

The output voltage is one of the major concern in an acid design. The flexibility of any asset chip can be improved by lowering the price of the device, lowering the mass, lowering the power consumption, and also reducing the complexity of manufacturing. The DSP blocks consume more amount of power where in the current ASIC design. The filter design of FIR user's residue number system rather than two complement number system. This helps in the reduction in the power consumption of for the system. The present research deals with the design of efficient, effective digital filters with the reduced utility of multipliers and adders, which in turn reduces the requirements of hardware, hence reducing the requirement of power and which impacts one minimized latency. In various applications of DSP viz., channel equalization, matched filtering, and pulse shaping due to the dependable stability and phase linearity. For designing arena of Filters of FIR kind can be broadly classified into two different categories such as few multiplier and sparse FIR, to attain the constraint of minimal hardware and less power is the highest design challenge. In the design aspect of the Filter in terms of the multiplier block, delay and SAs are considered for the various operators of the arithmetic to maintain the minimized area of operations which are essential for the DSP system. Hence it can be noted that FIR filters are considered as comparatively stable as it is operated the way that linear phase without any feedback. Conventionally all the coefficients of filter are expressed in integer and binary notations. The basic residue number system and its Major component blocks are shown in Fig.1.

[1]*Assistant Professor, Dept. of ETE, BMSCE, manjunathps.tce@bmsce.ac.in*
[2]*Department of ECE, Nitte Meenakshi institute of technology, Bangalore, sapnakumaricc@gmail.com*
[3]*Government Engineering College, Huvinahadagali - 583219*
[4]*Department of Computer Science and Engineering, Government Engineering College, Hassan, Karnataka, India, thirthegowda.gech@gmail.com*
[5]*Government Engineering College, Chamarajanagar, Visvesvaraya Technological University, Belgaum, ss.sharath@gmail.com*

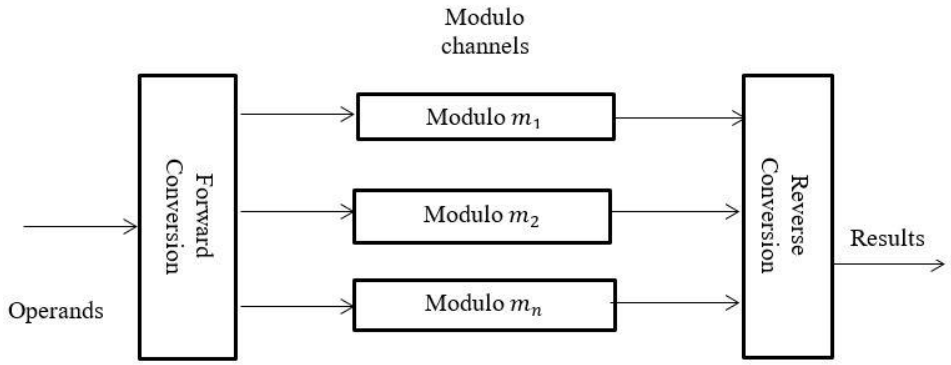

Fig.1: The basic principle of RNS

This paper is a small approach to understand the various applications that are carried out using modern VLSI design. Most of the applications are selected such that they are used for communication purpose with the help of Digital filter design. For the purpose of applications, the FIR filter is generally used in digital communication. The arithmetic circuits such as multipliers and adders are the main components of filters. The algorithm selection will results in the hardware requirement, power dissipation and also the delay aspects. The ultimate goal of this exercise east to reduce the hardware, lower the power consumption and also to improve the speed. This chapter completely deals with the different types of architectures and technologies used in the design of FIR filter. For the applications in the different regions, the FIR filter design is mainly used in the applications of the DSP. A filter design is structured using the RNS filter-based design, this was developed using the SDR filtration method used in the article. This also includes the concurrency and information in the process of clustering. In the specific application of FIR filter, the RNS provides the importance of statistics. Based on the numerous residue computations, the reverse translation has a significance mark. The expanded bit size in the results is the performance tradeoff in the conversely. Based on the replication of the RNS, the conditional delay are represented in the reverse process of optimization. This helps in the reduction of the FIR filter tradeoff for the future optimization device. The complete architecture is developed taking the base as distributed arithmetic algorithm. Based on the reverse translation, the store pre computational properties and the residual in the system architecture can be built using of RAM blocks. The complete structure is developed on FPGA devices. The processing latency of the delay and the performance torque, have increased appreciably when the proposed fire filter is implemented. The core benefits of RNS optimization algorithm is also explored in the structure. The complete structure is synthesized on the hardware FPGA with the input word size and also the length of FIR filter. The efficiency of the core filter is verified. The fetal audio signal detection is performed as the first step. From the experiment conducted, the results reveal that the optimization procedure followed when RNS methodology is implemented will compromise in the traditional FIR filters. The filter size is substantially decreased in the sophistication.

In [1], proposed and developed a Split Path Data Driven Dynamic Logic (SPD3L), which was considered as low power design of then. One of the subset of the input signals are global clock. This global clock is used in evaluation phase and recharge phases. Eradication of clock circuit would result in reduction of the power dissipation. The architecture in this paper users two 6x6 booth multipliers. These multipliers are designed with a CMOS technology using 0.18 micrometer and 1.8V. This will also use one normal SPD3L and the other set as the "Modified SPD3L". Based on the patterns of inputs, the proposed method in this paper will save the power in the slightest faster than the SPD3L technology. A new concept of analog multiplier with low voltage topology sis introduced by in [2]. A single low power supply is sufficient to drive the circuit. The complete circuit is made out of only 12 transistor. The sub circuits of the analog VLSI has a satisfactory need that is been accomplished. The power consumption of the circuit is comparatively less. The total harmonic distortion is found to be better than the previous models. In an example result, the following parameters were obtained: the power consumption of 130 uWatt when the power supply of 1.2 volts is used. The total harmonic distortion was found to be 1.1% in the bandwidth of 1 GHz. In [3] proposed an adaptive filter using for the approximation Distributed Arithmetic (DA) circuits, used in the fixed-point finite impulse response. The number of partial products in the Distributed Arithmetic circuit can be reduced to using Radix-8 Booth Algorithm, in the complete procedure there are no multiplication that are performed explicitly. By considering the error compensation, the partial products are approximately generated using the method of truncation. The Wallace tree is considered for the accumulation of partial product as a hardware. The proposed design gives a better system performance by reduced delay, reduced area and an appropriate power consumption. In [3] using the basic method of square

rooting circuit, a new four quadrant voltage mode analog multiplier was designed. The proposed circuit was capable of working at low power and also for low voltage applications. The reason it was able to work for low power and low voltage is it was using a flipped voltage follower cell. To design the circuit 0.18uM CMOS technology is used. The supply voltage of 1 V is used to operate the complete circuit. The differential input signal to the circuit was given as 40 mV. The worst-case power consumption of the complete circuit was measured to be as 4uW [4].

In [5] proposed a new high performance VLSI architecture. That is used to design a Least Mean Square Adaptive Filter using Distributed Arithmetic. A lookup table is designed to store the filter partial products. It also consists of a Shift Accumulator unit. In every iteration there is a calculation of address location of lookup table. Without the rotation of successive iteration, the updating strategy for the look up table has been designed. This helps to reduce the complexity of the design and also to increase the speed of computation. To store the offset binary coding, the lookup table utilizes the random access memory unit. The routing complexity in the circuit has been reduced and hence this helps in significant amount of architecture for the filter. In [6], proposed method to design a rounded, truncated hybrid multiplier. The maximum absolute error is calculated to be one unit less than the least position. To reduce the partial product, the full adders and the half adders are reduced. The reduction of full and half adders are included in the strategy of deleting the redundant partial product bits. The system is a high speed computation system which involves low power multipliers and high speed multipliers. To design the hybrid tree multiplier, Wallace tree and the Dadda method are combinedly used. The partial products in this method are separated into four different groups. To gain a better efficiency, the Dadda method is used in Group 1 and Group 4. Similarly, the Wallace tree is used in a group 2 and Group 3. In [7] proposed a new architecture to design DLL based frequency multiplier. This design is used for wireless transceiver. The proposed architecture occupied lowest area, consume the low power and low voltage with low phase noise. The DLL designs, our first order system. So the stability can be obtained in a better manner. The similar structure can be used to design a bigger multiplier for the desired reference frequencies. A suitably low supply voltage can be adopted to operate the circuit. For instance, it is considered that the multiplier was adopted to the 13 times of the reference frequencies. This paper presented a circuit level design. The power consumption tradeoff was also reported. The analytical predictions were is also shown in the results to confirm. There are several efficient multipliers built, these efficient multipliers also reduces the power consumption, the area and the delay of output generation. Chen et al., proposed a low power consumption multiplier. The author minimize the partial products by switching the application from boot technique to low power tools compliment multiplier technique. The radix for boot method is used to reduce the number of partial products in the activity of switching. In [8] multiplier was suggested with fixed width using left right technique. This is one of the downsides of fixed width multiplier method. The power dissipation of this method is comparatively high when compared with the cost. Still, it has an advantage of minimizing the partial product, that is, to improve the multiplication performance. In [9], proposed a design of linear array multiplier structure. This method is a result of combining several other technologies and methodologies. The drawback of this technique is it requires more space and the delay is more. But this technique is proved to be energy efficient when compared to other methods. There is a fair tradeoff between the parameters for the better result. In [10] proposed a method which is Suppresses the power dissipation using compaction tree. The booth decoder and the compaction tree of the multiplier are used to design the multiplier architecture. The resultant architecture consumes low power and also operates at a good speed. The architecture proposed consume higher area when compared to the other architectures. This is one of the major disadvantage of this design. In [11] proposed 2, 32 bit multipliers. These 2 multipliers are used to design them. Ripple carry adder and also a carry look ahead adder for combination. The resultant had a larger area, but it operated at a lower delay and also low dissipation of power.

2. Analysis of Problem in Fir Filter Design

The RNS and the DA have a greater issue to look into. Whenever the finite impulse response Filter is constructed using two different methods of DA and RNS, the results can be compared, to view which is the best technology. The frequency of the device is set to 500 MHz. According to the survey made, the RNS design should consume low power even at this frequency, and the size of the devices should not rise significantly. But every clock cycle the RNS and this year system must be able to interpret one signal and the receiver one signal. The main objective of the designed architecture is to process 20 bit of data. The conversions in the forward Conversion and the reverse conversion, will not provide much of the output area and power in the cognitive activity. The complete work concentrates on the results and the findings the goals archived for the technology. The design for the ASIC is used in 32nm technology. The complete circuit is designed on it. The immediate and interim goals, can be explained with the following criteria. RNS should show the superior performance in terms of area, power and timing than that of DA. To verify the technical choices, that are available for the RNS; the available options to enforce the technology. The additions that would help the

RNS for the better results in the qualities; the better ways and options in the RNS in the Ericsson's processes shown in Fig.2.

3. Proposed Rrns in the Fir Filter

The objective of the paper is to investigate the advantages and the strong points of the Adder and multipliers that are designed using the RNS architecture rather than that of others. The synthesis tool is given the liberty to select between the designs. The RNS specific methods consumes low power when compared with the existing methods. The total design of the FIR filter is made from the filter design. During the design of the RNS structure, the main concentration is done on the structure of the adder and the multipliers instead of the regular adders and the multipliers in the usage. Ericsson in Kista, Stockholm, was the site of the research project, shows the structure created in figure 5.1, the complete steps involved in the creation is mentioned below.

The literature of the research work is summarized as below. The adders and the multipliers are implemented using the RNS architecture; few of the comparisons are made using the RNS structures; the least power rated blocks of adders and the multipliers are compared, several other combinations are also verified in the same process.; FIR filters with the RNS and the DA blocks are implemented in the work.; DA and the RNS filter designs are compared in terms of the design aspects; to examine the various outcomes, the reverse and the forward implementation are implemented in the various ways of examining the outcomes.

3.1 The architecture of RNS arithmetic.

The basic RNS mathematics lies its foundation in algebraic symmetry correlation. Considering 2 integers as 'a' and 'b'. If the separation between a and b is considered as 'm'. the separation is said to be the number of the modulo (i.e. 'm'). The frequency of the theoretical situation is expressed by the equation a = b (mod m) . Let the division be 'q' and the residual be 'r'. When the integer is divided by the multipliers 'm'; the resultant is obtained as the a = q*m+ r. By using the compactivity equation used for the modulo we get it as a = r (mod m). the number 'r', is symbolized as the residual as the 'm'; this is rewritten as r= |a|m.

If 'r' is considered as the least set of positive characters in the modulo 'm', r€{0,1,2,…m-1}. Then 'r' is '0' for the set of LSB characters in the modulo. The created pair wise approximate moduli are $\{m_1, m_2,..., m_n\}$, with the moduli-set taking N positive number. The moduli of mj and mi are the moduli-set in the common divisor in the larger, for the each per j and I; in which i6 is considered as 'j'. the impedance is set for the RNS moduli, with the specific values of 'M'. as from the 'M', the moduli-set is defined as the equation (1).

$$M = \prod_{n=1}^{N} m_n (1)$$

Based on the every-moduli-set, the M integer has the N elements in independent discipline. The following equation is the determined by the following equation is $\{xi = |X|m_i : 1 \leq i \leq N\}$. The depiction is mentioned in the representation by the $(x_1, x_2, \ldots, x_N)$.

For considering as an instance: let the moduli-set is {3,5,7}; in the above equation the $m_3 = 7$, $m_2 = 5$ and $m_1 = 3$. The moduli for the dynamic-format speturm is shown as the $M = \prod_{n=1}^{3} m_n = m_1.m_2.m_3 = 3.5.7 = 105$. So, for the RNS moduli-set given as {3,5,7} can be represented as the (1,0,3). The values of the unsigned and the signed integers are represented in the number system. The RNS can promote for the unverified integer in the range of $0 \leq X \leq M - 1$, for the proposed unsigned numbers. The RNS, is used for the collection of the data in the equation in satisfy for the signed numbers as follows.

$\frac{-M-1}{2} \leq X \leq \frac{M-1}{2}$ if M is odd

$\frac{-M}{2} \leq X \leq \frac{M}{2} - 1$ if M is even

Table.1: considering the RNS is represented for the unsigned and signed numbers in the Moduli-set as the instance of the signed and unsigned for the expression given as $\{m_1, m_2\} = \{2, 3\}$, where M = 6.

(y_1, y_2)	(0,0)	(1,1)	(0,2)	(1,0)	(0,1)	(1,2)
Unsigned	0	1	2	3	4	5
Signed	0	1	2	-3	-2	-1

Selecting a Moduli-set: There are two groups, for the unique and generic ways. There are many particular in the moduli, that are employed in the special set of moduli in the 2^n-1,2^n,2^n+1. The other numbers now comprise of the integers and the unsigned multipliers. The relative prime numbers are entirely arbitrary moduli. The uncontrolled collections and the compromises of the integer will be claimed in this work. There are unique sets that compare

the even comparatives; these are hardware effective. For the status tickle standpoint that are simple, only the prime modulus and arguably are the best moduli-set and there are many unique sets.

The conversion system using moduli: Let us consider the system of modulis{m_1, m_2,…m_p}, Which are associated with the residues {r_1,r_2,…r_p}, These are related to the input operands as the equation mentioned below.

$$X = \sum_{j=0}^{4p-1} X_j 2^j = M_3 2^{3p} + M_2 2^{2p} + M_1 2^p + M_0 - - - (6.1)$$

Where $M_3 = \{X_{2p+k-1} \ldots . X_{3p}\} \quad for\ 1 \le k \le p \quad and\ M_3 = 0\ for\ k = 0$

Equation 6.1 shows the integer number in the binary form. This is used for the forward conversion of RNS system. The range of the integer X ranges from [0,N-1] The residuals of the equation will be as follows 2^{n-k}, 2^n, 2^{n+k}, The RNS set is $\{x_1, x_2, x_3\}$. The modeli set is { m_1, m_2, m_3} for the numbers as N= m_1*m_2* m_3.

The 2^{n-1} channel:

The residual channels that corresponds to the complex numbers are defined as 2^{n-1} and 2^{n+1}. This also depends on the final result which is of X bits. The area of the architecture is minimised and the speed of the computation is increased. The auditions are performed in a sequence, the equation through which the addition are calculated is as given below.

$x_1 = X_{2^n-1} = (M_3 2^{3p} + M_2 2^{2p} + M_1 2^p + M_0)_{2^p-1}$---- (6.2)

The other structure of equation 6.2 is:

$x_1 = (M_3 + M_2 + M_1 + M_0)_{m1}$ -------(6.3)

So by this we can conclude in the forward conversion, of x_1 to moduli 2^{n-1}. This can just be added by using modulo 2^{n-1}.

The $2^n + 1$ channel:

The identical procedure is performed to this residue operation also. The measurement of the residue is shown in the equation 6.4.

$$x_3 = X_{2^p+1} = (M_3 2^{3p} + M_2 2^{2p} + M_1 2^p + M_0)_{2^p+1} - - - (6.4)$$

The simplified form of equation 6.4 is as given below.

$$x_3 = (-M_3 + M_2 - M_1 + M_0)_{m3} \text{ ------(6.5)}$$

This helps in the performance of modulus and the commands identification within the appropriate range. The dynamic range is calculated before the measurements. The removal of modulo is conducted when both the section equations 6.5.

The basic function of the FIR filter is given by the equation.

$$y(z) = \sum_{j=0}^{M-1} x(j)h^{-j} = \sum_{j=0}^{M-1} x(n)h(n-k) - - - -(6.6)$$

In the ever equation, the value of key is the length of the filter. The range of key is from 0 to 63. The above equation represents the direct FIR Filter. This user sphere registers as shown in the figure 6.2. The residue number system based RF is shown in the figure 6.1.. The coefficients of module order and the standard FIR filter architecture in the binary number scheme is represented. The greater diffusion and the net weight of the restricted speed activities is mentioned here. To overcome the drawback, the RNS number system is implemented for FIR filters. This helps in the fast modification of parallel prefix adder. This avoids the propagation delay of carry bit. This is nothing but the modified parallel prefix adder as mentioned in table 6.1.

The structure of FIR filter: Filters are often used to remove unwanted frequencies of the signal. Digital filters are used for finite duration impulse response. To determine the output of an FIR filter, The expression is shown in the equation (2). The discrete multiplication is the theoretical notion to construct the FIR filter.

$y[n] = \sum_{i=0}^{N} h[i]x[n-i]$(2)

The output is represented as y[i], the input is x[i] and the coefficients of the filters are represented as h[i]. To define the filter order, the notation used is ‘N’. The Fig.2 shows the N taps that are present in the filter design.

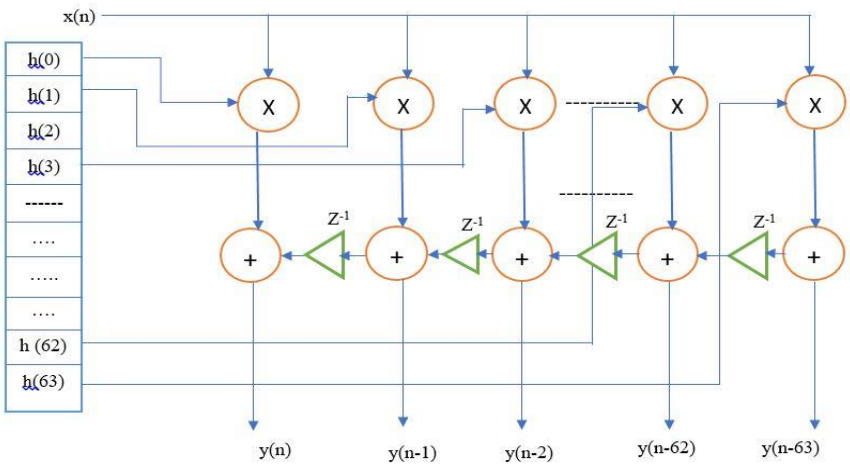

Fig. 2: The interior structure n_i^1 of suggested subband information response filter.

The steps to design: there are 4 simple steps involved in developing of a filter. The step one was resumed for any error occurred in any of the stage.

- Implement the filter.
- Duplicate and replicate the current situation and compare the output results to the DA based multiplier.
- Synthesize.
- Comparing the profiles like area, strength and latency to analyze the composite effect.

4. The Arithmetic Functions Involved in the Fir Filter

The addition and the multiplication are the basic operations of any sort of filter. Including FIR filter, these are the 2 main operations that are done on the obtained attack. Using varieties of method in RNS system, the procedures are accomplished. The most basic operations with RNS modulo exist. Whenever the result exceeds modulo. The output range of the procedure should always lie in the modulo mi; the range is specified as {0,..., m_i-1}. It is known that the output of the audition will be in the range of {0,..., 2(m_i-1)}. But the subtraction range with mi will vary. The range of the result if the multiplication operation is done is given as $\{0,\ldots,(m_i-1)^2\}$. This makes the reduction still more difficult. To perform the determined operations such as multiplication and addition, analysed and specific multipliers and also specific adders are chosen for the moduli. This helps to get the overall best output voltages.

Addition: There are 3 ways to develop the arbitrary modulo additions. The lookup tables 2 conventional binary adders and the combination of these 2 technologies are the 3 main methods that can develop the addition module. For the given modulus, we can have 3 options that are best in terms of duration and also best in terms of space, present more unique way that uses the parallel prefix adder to perform the addition even in the peculiar modulo set$\{2^n-1, 2^n, 2^n+1\}$. A complete explanation is found in the paper. Another technique is proposed, that user starting the deployment concept of low level. The Verilog language has 2 inbuilt operators that are used in this coding. They are the addition operator '+' and the modulus operator '%'. These 2 operators are also supported by the generation engine. For a good Navi baseline at this method is solely used for evaluation of other methods. The utilization of simple normal adders along with the utilization of modulo2^n. The following are the steps used to implement the addition operation in this work.

- The RNS operation, based on the lookup table.
- Binary adders in 2 number count.
- The hybrid model that connects between the second step and the first step.
- Modified parallel prefix adder that implements Modulo 2^n-1
- Usage of 1D representation using Modulo 2^n+1
- Usage of modulo 2^n, for adder.

Multiplication: Varieties of methods are used to express the multiplication that is based on RNS combination. A modulo-m product spitting multiplier that uses ROM is one of the possible methods that is proposed in [15]. In this method, 3 multipliers are involved, whereas in the normal multiplication only 2 are involved. This method is more feasible for energy efficient multiplication and also it is equal to the modulus Operation as reported in [17]. There are some enhancement done in terms of energy, latency and the distance. The enhancement is done using the unique set $\{2^n-1, 2^n, 2^n+1\}$. A parallel modulo M multiplier is the present in [16] that is used for the multiplier for 2^n+1. This doesn't require any sort of speed up approach. And is represented in Fig.3.

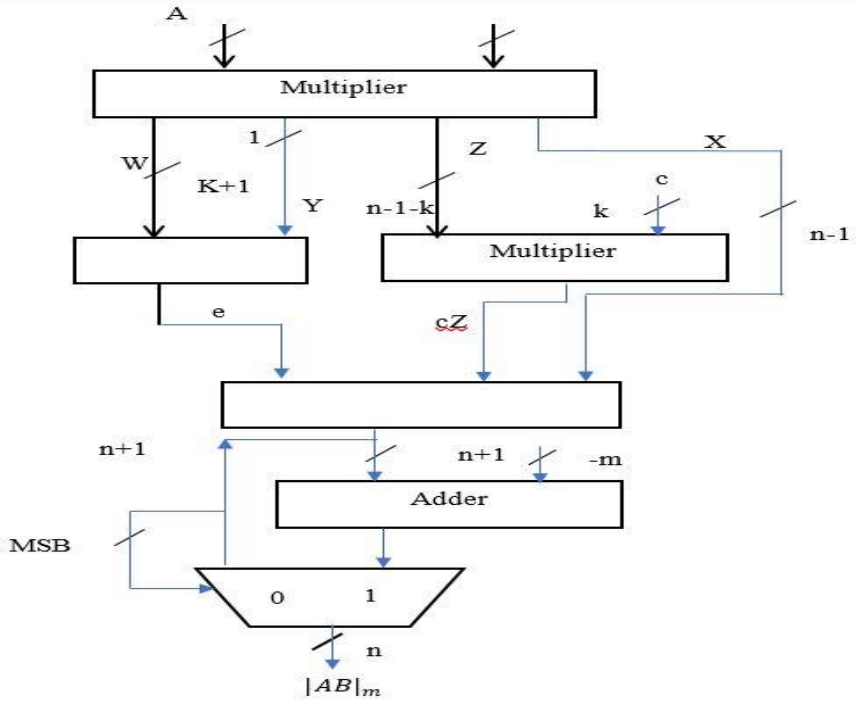

Fig.3: Block diagram of Modulo-m product-partitioning multiplier that users ROM

This approach is used only when the number of taps are small, that is 'n'. The booth-8 encoding algorithm is used to implement the multiplier for $2^n + 1$. This technique is well suited for n=32 rather than other methods. This also can be used for the values which are lower 'n'. If this was not the situation, the booth-4 encoding can also be used. RNS users, most of the boot encoding in its implementation. So this might not be a proper exploration to this work. An integrating method was proposed (Jassbi et al., 2010), This country plays the multiplication with the addition operation. The lookup tables are used with an isomorphic technique. The bustle still remains to see how the implementation can be done.

Forward conversion: Reversal translation is little difficult when compared to the forward translation for the accomplishment. In spite of the fact of the residue number system that must be able to represent the specific number of bit width, whenever the input is generally considered as a smaller bit with the number, this method can be used. Anyhow this decreases the amount of difficulty. The forward conversion problem can be solved, by following the well-known formula to calculate the RNS number using the equation (3)

$$-a_{n-1} - 2^{n-1} + \sum_{i=0}^{i=n-2} a_i\, 2^i \quad (3)$$

To find the sum of $a_i 2^i$, it is better to use RNS adder instead of PPA adders. This is one of the easiest approach to solve the algorithm. By making small changes in the input, negative numbers can also be handled. As a technique of tweak the cyclical quantities of modulus can also be used for the implementation. The periodic characteristics can be obtained by using the Residue of each 2^i mod m. There is a lookup table, best solution possible. Whenever the input contains all conceivable input combination. The input combinations can be from n_{input} bits. This corresponds to the value of RNS when $n_{rns} \geq n_{input}$ bits.

As a part of result, this is this approach can be further ruled out in the research. There is a modular exponential technique that has been proposed in [18], this technique is most interesting. It is one of the most sophisticated and parameterized implementation for modulo arbitrary input width that are extremely challenging. There are few sequential algorithms that are proposed, but they are not expecting to get a good result.

Reverse conversion: The reverse translation is a process of converting the RNS system to FIR system. The Mixradio conversion are the 2 basic approaches that are used for the translation purpose. The CRT method is the simplest among all the options available. The mixed radix technique that is used in mercy will result in most of the research works. There are few other alternative approaches like a pseudo SRT division. This is one of the most famous method to convert and is also an efficient algorithm. The core function mentioned in (Goel & Nandi, 2015). These methods also use the lookup tables that are instrumenting methods. When the lookup tables are used, There is a lot of work handled by the synthesis tool to solve the issue.

Selecting a modeli-set: If the filter is considered with large number of taps. The percentage of power dissipation still occurs during the ordinary operations also. This is also measured in forward and reverse transformation. Just

results in the contradiction of the primary assumption made for the moduli set, that is by comparing the output power of a simple tap element with the large tap elements. For this reason, the basic component should be ideally constructed for the filter structure. So the components are constructed in variety of ways before an ideal way. And near optimal or the optimal arrangement is a determined and accordingly the design of the architecture is made.

Parallel-prefix adder using end/around carry: This is used to function only for the carry parallel prefix adder that functions with modulo 2^n-1, this can be used for the same regular parallel prefix adder. This also uses the end around carry condition. Whenever the number is converting the RNS and into the VHDL form. It uses system Verilog for the conversion and the parallel prefix adder is created. Sklansky parallel-prefix structure, is employed to create the end around carry condition. The Fig.4 represents the added employed for variety of logical operators. The exact behavior of the architecture is described by the equation as a logic process.

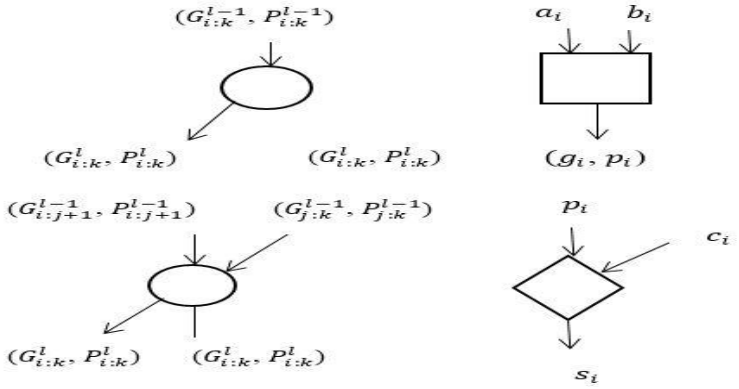

Figure 5.4. Logic operators for the parallel-prefix adder

5.5 PROPOSED RFIR FILTER DESIGN USING RNS AND PPA

To complete the operation of equation 2. Some of the familiar features are used to implement. This is shown in the Fig. 5 and also by 3 in the concept of variety of approaches. A small technique that shows the shifting of the register before the multiplication operation is done in the summing change is represented in the Fig.5. This can enhance the device output significantly. This is it, also defined as the transposed of direct from one of FIR filter. This design has a bigger area when compared with the direct form FIR filter structure. But for time being, the considerations are made only for the addition and multiplication. For comparison sake. The simulation of this theses was done using the transpose direct form FIR filter as illustrated in the Fig.6.

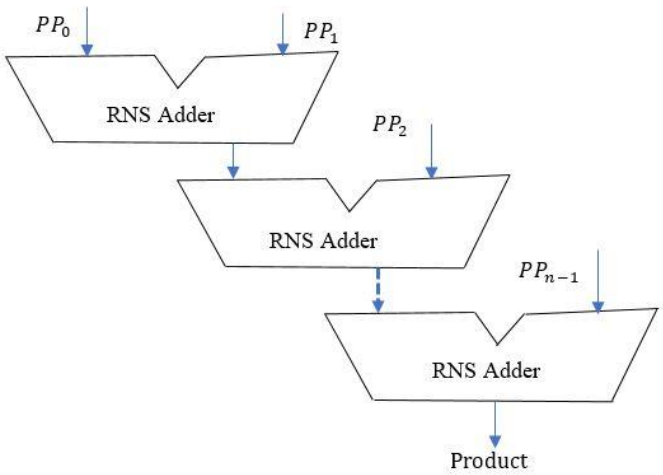

Fig.5. Multiplier based on parallel-prefix RNS adders

Based on the multipliers proposed. The high radix modular multiplier of RNS is considered for modulo 2^n - 1. Another modulus $\frac{n-1}{k}$= 4, function is introduced as a multiplier in [19]. This helps in the integer and the number of bits necessary to represent modulo 2^n -1, and the n-1 values respectively. The basic assumption of this structure is the multiplier can multiply the values of input as sum of partial products. Add the initial stage, the values of multiplier and multiplicand is divided into 2 k-bit numbers which are represented as follows.

$$K = \frac{\log_2(2^n-1)+1}{2} \qquad (4)$$

so that $A = A_1 2^k + A_0$ and $B = B_1 2^k + B_0$

Now the product $A \cdot B$ can now be rewritten as equation (4.8) by using cyclic convolution.

$$P \cdot Q = (P_1 2^k + P_0).(Q_1 2^k + Q_0) = 2^k(P_1 Q_0 + P_0 Q_1) + (P_1 Q_1 + P_0 Q_0) = 2^k A_1 + A_0 \qquad (5)$$

This can be extended to $|P \cdot Q| \quad |P.Q|_{2^n-1} = |2^k A_1 + A_0|_{2^n-1}$ for modulo 2^{n-1}.

A_0 and A_1 can also be expressed as

$$A_0 = \frac{a^2 - b^2 + c^2 - d^2}{8} \qquad (6)$$

$$A_1 = \frac{a^2 - b^2 - c^2 + d^2}{8} \qquad (7)$$

Where,

$a = P_0 + P_1 + Q_0 + Q_1$

$c = P_0 + P_1 - Q_0 - Q_1$

$d = P_0 - P_1 + Q_0 - Q_1$

$b = P_0 - P_1 - Q_0 + Q_1$

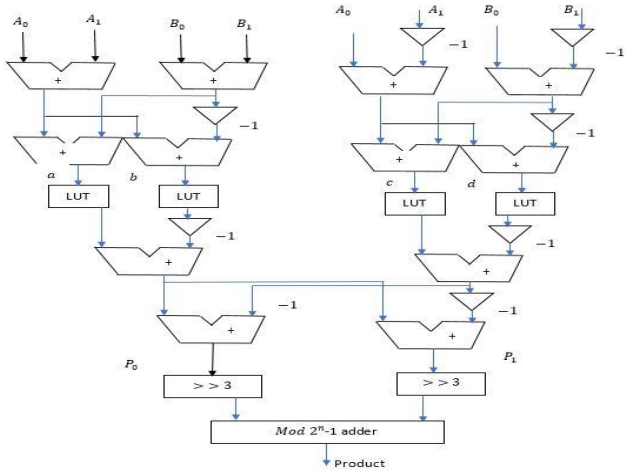

Fig.6. Modular high-radix RNS multiplier

5. Results and Discussions

There are various set of moduli that are used in this experiment to find the FIR filter design. The Verilog HDL code is used to create the path, position and the propagation of digital strategies. The compatibility of the code and using the Modelsim simulator and the calculation of metrics is also analysed using the FPGA hardware. The FPGA hardware used in this work is Artix-7. The summary of the work is mentioned in Table 5.3 and the table 5.2. Assuming the design is based on the speculation distributed arithmetic algorithm. The delay limitation has been a greater effort. The dominance of the theoretical DA based RNS framework in different dynamics of FIR filter is presented by assessing computation upstairs as theoretical results exploitation through hardware implementation with simulated results are as shown in Fig.7.

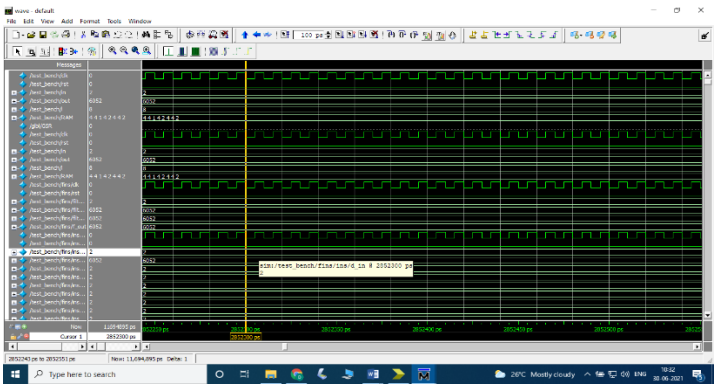

Fig.7. Proposed simulated RNS based FIR filter results

Table.2. Optimization synthesis results for different input block size

Input word length size		Existing	Proposed
		16 bit	32 bit
Moduli set (2^n+1,2^n,2^n-1)		(7,8,9)	(41,42,43)
RNS and conventional RNS computation	**Area (LEs)**	3821	5439
	Fmax	184.34MHz	253.325MHz
Speculation and RNS	**Area(LEs)**	2729	7631
	Fmax	179.48MHz	328.78MHz

Table. 3. Comparison between RNS based FIR design. [ADP: Area-delay product] and [PDP: Power-delay product]

Method/Parameters	Existing (Kumar & Rangaraju, 2021a; Kumar et al., 2020)	Proposed
Slice Registers	1311	155
FF's	543	155
Slice LUT's	14445	102
Delay	13.76ns	3.947ns
Power (Watts)	2.672	0.082
Frequency	184.34MHz	253.325MHz
ADP	20011	6117
PDP	11.48	3.23

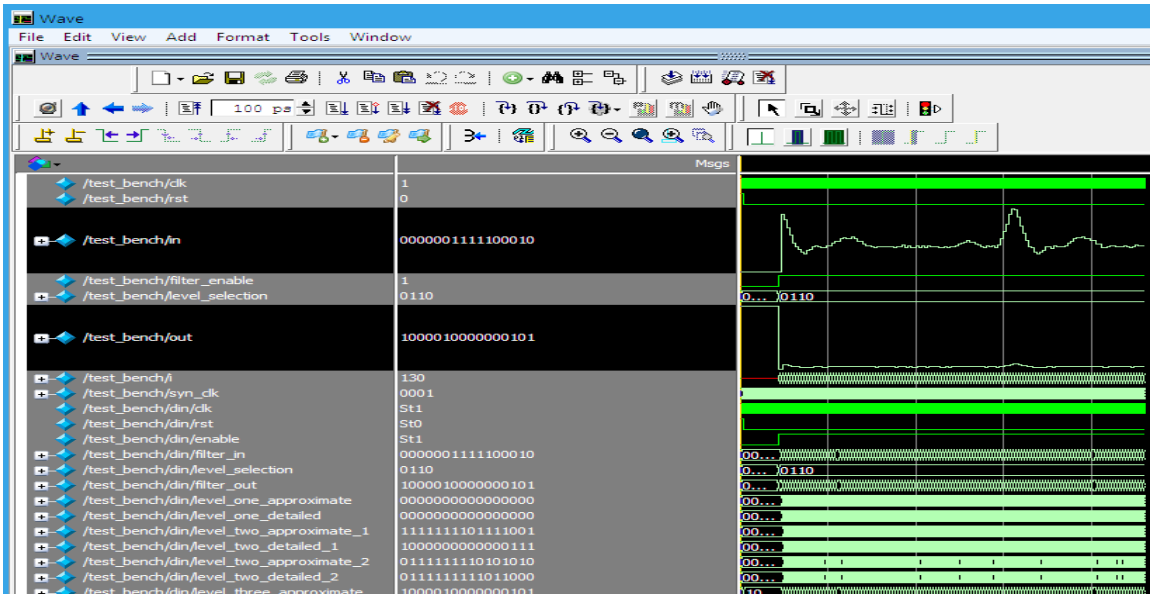

Fig.8 Audio samples were extracted, and the simulated data was filtered afterward

The Fig.8 uses introduction is done using the technique to confirm that the reliability and functionality of the design with long length word. The result shows the high position transfer function with enhanced carrier frequency and reliable processing are used for filtering methods

6. Conclusion

Based on the huge research where the iron is may be evaluated for the advancement. In the digital signal processing area, there are several implementations that have been suggested at the same time. The analysis of RNS helps in reduction of power dissipation even more. The observations made during the exploration are noted down here. For the modulus 6=2n, none of the simulation are the import combinations have been explored. So RNS implementation also have a supplementary level for this research. And the suggestion of RNS architecture for this implementation is probably better. There are several researchers carried out for the larger models, including RNS for supplementary levels. The bit word of the RNS architecture is substantially larger when compared with the other research work. In this work at the multilevel RNS architecture has been used. Because of the inherent features, there are similar arithmetic algorithms have been explored in RNS algorithm, even for small world length. One example has been instantiated in the above using shift and add multiplication. The powerful add a tree structure might also be possibly re implemented using parallel prefix multiplier. There are so many unique arithmetic algorithms. There are explored to inherit the features of small world length to RNS architecture. The useful thing in the complete design is to optimize the modulus set. Furthermore, the advanced study on forward and reverse conversion is very much necessary, If the real time system need to be implemented using RNS. Scaling analysis, overflow analysis, and others are certainly done to compensate the conversion process. This research article introduces a systematic study of various types of 2n-1 module without memory, and is tested by forcing the Booth algorithm, which improves the efficiency of the 2n-1 module coefficients by limiting the number of PPs, limited by one-third of coefficients with a codex radius-8 Booth-encoded Due to the presence of Hard-multiple, this multiplier does not work in small ranges, but is highly developed in terms of strength and region in large dynamic widths. To avoid the problem of intra carry transmission, the residue number system is suitable for dynamic range, along with the madhilo converter. There is a still space for research in the field of 2n-1 modulo. There is also a future work to update the boot encoding converter for higher radix. The RNS system can be used to achieve the important model converter in the DSP. The fetal analysis of ECG signal the above investigation can be involved. The hardware is also optimized in an effective way, whenever the RNS computation has detected. The efficiency penalty gap between the FIR filter is reduced by using RAM based theoretical reverse transformation and the best residue estimation. By the integration of Mac based system and also memory efficient reversible converter unit. This work restores the reliability of the performance of filter.

References

[1] D. Pakiyarajah and C. U. S. Edussooriya, "Minimax Design of Computationally-Efficient FIR Graph Filters Using Semidefinite Programming," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 9, pp. 3655-3659, Sept. 2022, doi: 10.1109/TCSII.2022.3181540.

[2] A. L. Jayaweera, D. Pakiyarajah and C. U. S. Edussooriya, "Minimax Design of M-D Sparse FIR Filters With Arbitrary Frequency Response Using SOCP," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 5, pp. 2403-2407, May 2022, doi: 10.1109/TCSII.2022.3160400.

[3] M. Kumm, A. Volkova and S. -I. Filip, "Design of Optimal Multiplierless FIR Filters With Minimal Number of Adders," in IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 42, no. 2, pp. 658-671, Feb. 2023, doi: 10.1109/TCAD.2022.3179221.

[4] M. D. Kušljević, "IIR Cascaded-Resonator-Based Filter Design for Recursive Frequency Analysis," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 9, pp. 3939-3943, Sept. 2022, doi: 10.1109/TCSII.2022.3172245.

[5] S. H. You, C. K. Ahn, S. Zhao and Y. S. Shmaliy, "Frobenius Norm-Based Unbiased Finite Impulse Response Fusion Filtering for Wireless Sensor Networks," in IEEE Transactions on Industrial Electronics, vol. 69, no. 2, pp. 1867-1876, Feb. 2022, doi: 10.1109/TIE.2021.3055172.

[6] S. Afrandideh, "A Modified DFT-Based Phasor Estimation Algorithm Using an FIR Notch Filter," in IEEE Transactions on Power Delivery, vol. 38, no. 2, pp. 1308-1315, April 2023, doi: 10.1109/TPWRD.2022.3213247.

[7] L. Ben Saad, B. Beferull-Lozano and E. Isufi, "Quantization Analysis and Robust Design for Distributed Graph Filters," in IEEE Transactions on Signal Processing, vol. 70, pp. 643-658, 2022, doi: 10.1109/TSP.2021.3139208.

[8] E. G. Pale-Ramon, Y. S. Shmaliy, J. A. Andrade-Lucio and L. J. Morales-Mendoza, "Bias-Constrained H_2 Optimal Finite Impulse Response Filtering for Object Tracking Under Disturbances

and Data Errors," in IEEE Transactions on Control Systems Technology, vol. 30, no. 4, pp. 1782-1789, July 2022, doi: 10.1109/TCST.2021.3118321.

[9] L. Chen, X. Xie, M. Song, Y. Li and Y. Zhang, "Estimation of High-Frequency Oscillation's Magnitude and Frequency Based on Multi-Tone FIR Filter," in IEEE Transactions on Power Systems, vol. 38, no. 1, pp. 528-536, Jan. 2023, doi: 10.1109/TPWRS.2022.3155630.

[10] J. Guo, P. Yu, Y. Li, Y. Song and F. Jing, "Optimal Preiod Input Design in FIR System Identification with Binary-Valued Observations and Event-Triggered Communication," in IEEE Transactions on Circuits and Systems II: Express Briefs, doi: 10.1109/TCSII.2022.3223967.

[11] Y. Huang, S. Che, G. Zheng, W. Zhu, Y. Zhou and Z. Xue, "An Adaptive Filter for Subdivision of Circular Grating Signal of Angle Measurement," in IEEE Transactions on Instrumentation and Measurement, vol. 71, pp. 1-10, 2022, Art no. 9511410, doi: 10.1109/TIM.2022.3192068.

[12] J. A. Ortega-Contreras, Y. S. Shmaliy, J. A. Andrade-Lucio and O. G. Ibarra-Manzano, "Robust H_{2}-OFIR Filtering: Improving Tracking of Disturbed Systems Under Initial and Data Errors," in IEEE Transactions on Aerospace and Electronic Systems, vol. 58, no. 5, pp. 4761-4770, Oct. 2022, doi: 10.1109/TAES.2022.3155588.

[13] Z. Li et al., "Adaptable Approximate Multiplier Design Based on Input Distribution and Polarity," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 30, no. 12, pp. 1813-1826, Dec. 2022, doi: 10.1109/TVLSI.2022.3197229.

[14] L. Li, P. Shi and C. K. Ahn, "Distributed Iterative FIR Consensus Filter for Multiagent Systems Over Sensor Networks," in IEEE Transactions on Cybernetics, vol. 52, no. 6, pp. 4647-4660, June 2022, doi: 10.1109/TCYB.2020.3035866.

[15] Y. S. Shmaliy, Y. Xu, J. A. Andrade-Lucio and O. Ibarra-Manzano, "Predictive Tracking Under Persistent Disturbances and Data Errors Using H_2 FIR Approach," in IEEE Transactions on Industrial Electronics, vol. 69, no. 6, pp. 6121-6129, June 2022, doi: 10.1109/TIE.2021.3087403.

[16] H. Wang, W. Xu, Z. Zhang, X. You and C. Zhang, "An Efficient Stochastic Convolution Architecture Based on Fast FIR Algorithm," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 69, no. 3, pp. 984-988, March 2022, doi: 10.1109/TCSII.2021.3121081.

[17] Moir, T.J. (2022). FIR Filter Design. In: Rudiments of Signal Processing and Systems. Springer, Cham. https://doi.org/10.1007/978-3-030-76947-5_8

[18] Oppenheim, A.V., Schafer, R.W.: Discrete-time Signal Processing. Prentice Hall, Englewood Cliffs (2009)

[19] Rabiner, L.R., McClellan, J.H., Parks, T.W.: FIR digital filter design techniques using weighted chebyshev approximations. Proc. IEEE **63**(4), 595–610 (1975)

.