International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Design of MPA Array with Wilkinson Power Divider for Improved Characteristics

B. Ashok Kumar[1], P. Mallikarjuna Rao*[2]

Submitted: 29/01/2024 **Revised**: 07/03/2024 **Accepted**: 15/03/2024

Abstract: In this paper, an 8-Element MPA array is designed for X-band frequency at 9.1GHz with corporate power divider and then Wilkinson power divider is placed at the first stage to improve the array over all characteristics. The first side lobe level of the array has been decreased from -13.26dB to -16.48dB and the front to back ratio is also increased from 19.59dB to 24.63dB due to combined effect of corporate and Wilkinson power dividers. The overall gain of the antenna has not deteriorated although the radiation efficiency is slightly decreased. In this work, FR4 substrate is considered with thickness h=1.60mm and ε_r =4.40.The simulations are carried out using HFSS and the important parameters namely return loss, VSWR and Gain are measured by using vector network analyzer.

Keywords: *parameters, FR4, MPA, VSWR, Wilkinson, deteriorated, substrate*

1. Introduction

For array of microstrip antennas with suitably great gain, lower SLL, narrow beamwidth, and high front-to-back ratio are the desirable features which pose challenges for designers. Gain implemented has been done by increasing the numerical strength of array elements; however reduction of SLL and increase of front to back ratio have been defying proper solution so far.

The method of insertion of slots in the central portion as well as on the edges with no radiation for the patch antenna has been proposed to improve the gain and decrease the side lobe level [1]. CSRR amplitude processing technique has been proposed for side lobe reduction of planar array antenna in [2]. In [3], the idea of a non-identical structure with a cosine square pattern over pedestal pattern has been suggested for microstrip array of antenna. This is applicable for reducing side lobe on X-band. The technique of asymmetrical placing of elements has been suggested for improvement of front to back ratio [4]. The technique of placing parasitic metallic rods on either side of the microstrip patch antenna for improvement of front-to-back ratio is proposed in [5]. Furthermore, the method of placing semi-cylindrical side walls at the edges has been proposed in [6] for the same ratio improvement. It is pertinent to note that all these methods are not easy for implement. More or less all these techniques are difficult to implement. In this work, a very simple technique is presented for simultaneous reduction in side lobe level as well as improving the front-to-back ratio. By placing the wilkinson power divider at the first stage of corporate power divider, both side lobe level reduction and improvement in front to back ratio is achieved for 8 element linear array of microstrip antenna. The design antenna is for 9.1GHz using FR4 substrate is used here and HFSS has been used for simulation.

2. Design of Wilkinson Power Divider

It is worth noting that the wilkinson power divider comprises line of transmission that can be split into many lines of length for giving isolation amongst ports of output [7]. From the fig 1 showing the equivalent diagram, the power at two ports is found to be identified.

In the original suggestion of wilkinson, a plates for shorting at the input for connecting the lines of transmission. Further resistors are put between each output line of transmission and a central junction. For an equal split case of wilkinson, the two outputs are connected for matching loads so that voltages at the lines of transmission are of the same magnitude as well as phase. The result is that connecting resistors do not have voltage drops and hence there is no dissipation of power [8].

Furthermore, the ratio of the impedance of the quarter wave line to the characteristic impedance of the input line of transmission is . The internal resistor connected between the ports of output is twice the characteristic impedances of input line (fig 2). For 50Ω input, the value of the corresponding resistor is 100Ω. It may be noted that for such values, the output ports are having isolation as well as matching. No output is discovered at port 3 when input is applied at port 2.

[1] *S.D.M.College of Eng. &Tech, Fort Collins – 8023, USA*
ORCID ID : 0000-3343-7165-777X
[2] *KLE.Institute of Technology, Tsukuba – 80309, JAPAN*
ORCID ID : 0000-3343-7165-777X
[3] *Computer Eng., Selcuk University, Konya – 42002, TURKEY*
ORCID ID : 0000-3343-7165-777X
** Corresponding Author Email: author@email.com*

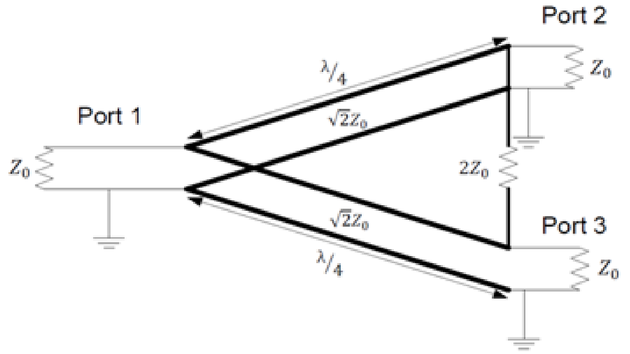

Fig.1. Transmission line circuit model for wilkinson power divider

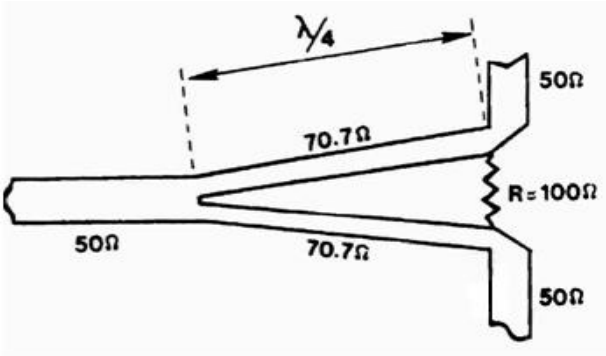

Fig.2. Wilkinson power divider for 50 ohm input

Figure 3 shows the schematic view of the divider and Figure 4 represents the plot of s-parameters. Both S_{12} and S_{13} are around -4.03dB at 9.1GHz. Theoretically, it should be -3dB. The deviation is due to losses at discontinuities. S_{11} of -13.98dB and S_{23} of -14.4dB are observed at 9.1GHz. Good isolation is achieved between port 2 and port 3.

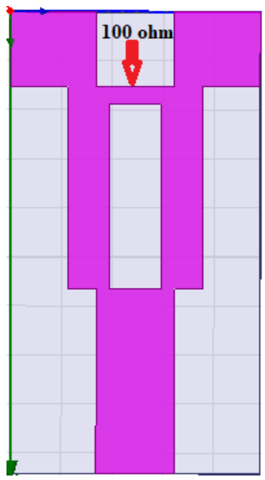

Fig. 3. Schematic view of wilkinson power divider

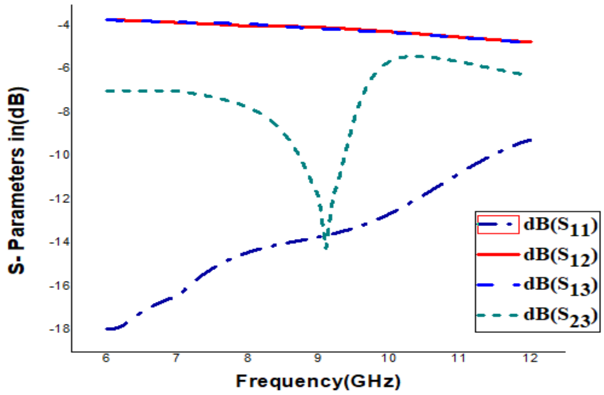

Fig. 4. S- Parameters plot of wilkinson power divider

3. Design of Uniform 8 Element Linear Antenna Array

At first, the single microstrip design is made at 9.10GHz and then it is optimized for better return loss. The following design equations are utilized for making the microstrip structure with edge feeding [9].

The substrate FR4 used here, with thickness h=1.60mm and εr=4.40 is chosen. At resonant frequency fo= 9.1GHz. Width "W" is determined as follows [10].

$$W = \frac{c}{2f_0\sqrt{\frac{(\varepsilon_r+1)}{2}}} \quad (1)$$

The patch effective length is given by

$$L_{eff} = \frac{c}{2f_0\sqrt{\varepsilon_{reff}}} \quad (2)$$

ε_{reff} is effective relative dielectric constant

C represents velocity of light (3x10^8 m/s) and ε_{reff} is given by the following equation

$$\varepsilon_{reff} = \frac{\varepsilon_r+1}{2} + \frac{\varepsilon_r-1}{2}\left[1+\frac{12h}{w}\right]^{-\frac{1}{2}} \quad (3)$$

The electric fields at the patch edges have been effects of fringing which makes the effective length appropriately higher than the real value. Hence the actual & effective length can be expressed as

$$L = L_{eff} - 2\Delta L \quad (4)$$

Here, ∇L gives a function of ε_{reff} for w/h.

$$\frac{\Delta L}{h} = 0.412\frac{(\varepsilon_{reff}+0.3)}{(\varepsilon_{reff}-0.258)}\frac{\left(\frac{w}{h}+0.264\right)}{\left(\frac{w}{h}+0.8\right)} \quad (5)$$

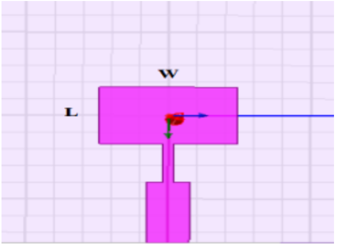

Fig.5. Microstrip line fed rectangular patch antenna

Width is W=10.05mm, length is L=7.19mm. Keeping W fixed and varying the length, the MPA is in turn improved for better return loss. At L=7.124mm return loss of -35.72dB is obtained using optometric analysis in HFSS. The optimal values of rectangular shape is W = 10.05mm and L = 7.124mm.

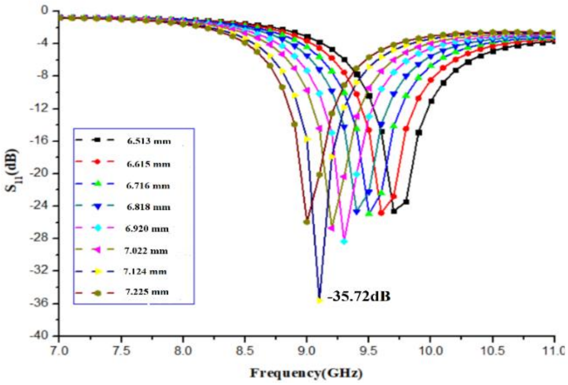

Fig.6. S_{11} plot of single patch antenna for L variations

These final dimensions of patch antenna are used in constructing the 8-element linear array antenna. The array antenna is implemented with corporate power divider. Quarter wave transformer rule is used in these power dividers [11].

The impedance of quarter wave transformer Z_2 is given as geometric mean of two impedances Z_3 and Z_1.

$$Z_2 = \sqrt{(Z_1 Z_3)} \qquad (6)$$

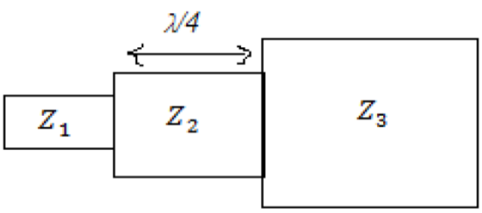

Fig.7. Quarter wave Transformer

Using the corporate feed technique a linear 8-element patch array is designed as shown in Fig. 8. From the 50Ω line power is fed and divided equally into two sides using 100Ω lines and again 100Ω line is joined to a 50Ω junction point using a quarter wave transformer impedance of 70.70Ω. This is repeated for the next stage. The patch impedance is 251.9Ω. In the last stage patch and 100 Ω line are joined using a quarter wave transformer of 158.7 Ω for impedance matching. The final dimensions of the strip lines are given in Table 1.

Table1. Corporate power divider dimensions

S.No	Impedance (Ω)	Length (mm)	Width (mm)
1	50.00	7.53	3.06
2	70.70	4.63	1.62
3	100.00	Variable	0.71
4	158.70	4.87	0.14

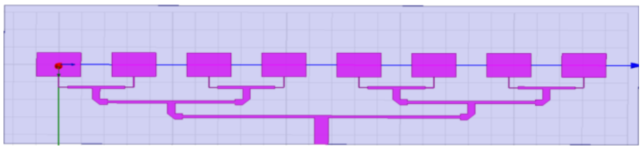

Fig. 8. Eight element linear array with corporate feed network

4. Design of Antenna Array with Wilkinson Power Divider Placed at First Stage

The designed Wilkinson power divider in the above section 2 is placed in the first stage of the corporate power divider to improve the array characteristics. Placing the Wilkinson power divider in the next two stages would result in poor design of the array because of the increased size and complexity of the array. Figure 9 shows the design array with the Wilkinson power divider. Measurement is carried out for Wilkinson power divider for removal of reflections at the bands as well as reduction of impedance mismatching [12].

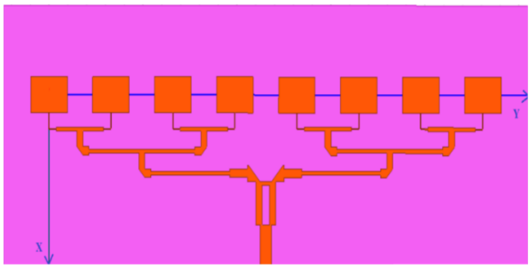

Fig. 9. Eight element array with Wilkinson power divider

5. Results & Discussions

Fig 11(a) & 11(b) depict 3D gain polar plots of the array in two cases. Peak gains of 12.03dBi and 12.30dBi are obtained respectively in these two cases. A gain bandwidth of 986MHz is observed in the case of an array with a corporate power divider and it is 971MHz with a modified power divider. The first side lobe level has decreased from -13.26dB to -16.48dB when the Wilkinson power divider is introduced. The second and higher-order side lobe levels are much decreased compared to the side lobe levels in the case of an array with a corporate power divider. It can be observed from Figure 13. The front-to-back ratio has increased to 24.63dB from 19.59 dB. The radiation efficiency has slightly decreased from 59.64% to 56.78%. Table 2 gives the performance comparison of the array with two different power divider networks. Figure 17 shows the return loss comparison plot of the array with the Wilkinson power divider. A deviation of 1.9dB is observed between measured and simulated return loss at 9.1GHz. Figure 18 shows the plots comparison of measured and simulation results of the VSWR plot of the array with the Wilkinson power divider. Figure 19 shows the measured VSWR value of the array at 9.1GHz for the proposed antenna array. Figure 10 gives the comparison of the return loss plot for the array in two cases. The return loss of -15.60dB is observed at 9.1GHz in the case of an array with corporate power divider and it is -13.27dB with Wilkinson and corporate power divider.

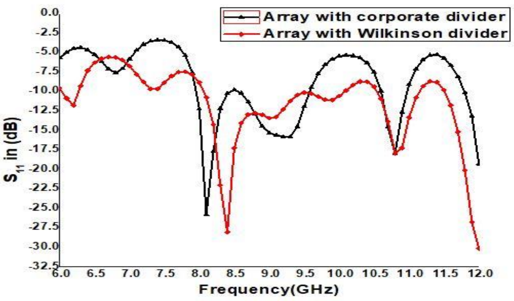

Fig. 10. S_{11} Comparison plot in case of two different feed networks

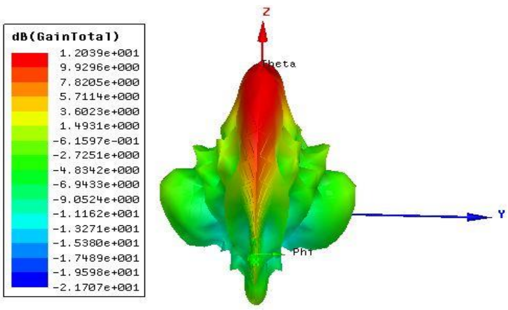

Fig. 11(a). 3D gain plot for 8-element linear array

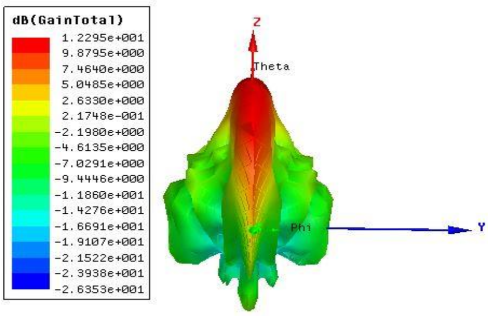

Fig. 11 (b). 3D Gain polar plot of the array with Wilkinson power divider

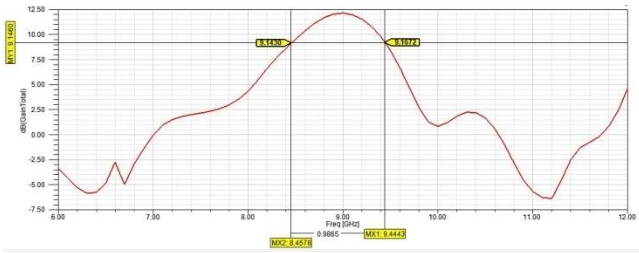

Fig. 12(a). Gain versus frequency plot for 8-element array with corporate feed

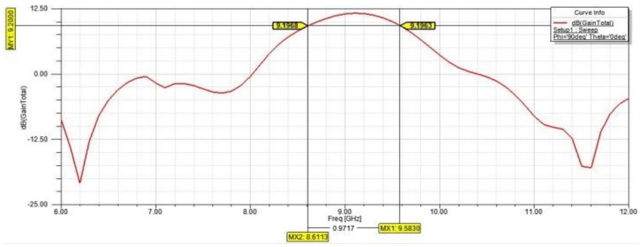

Fig. 12(b). Gain versus frequency plot for array with Wilkinson power divider

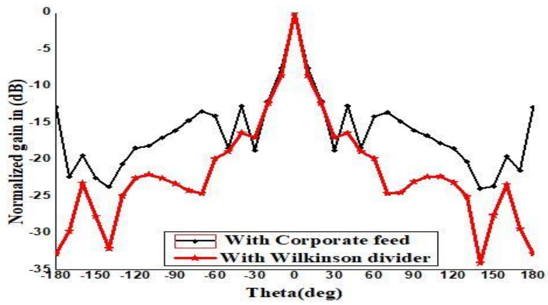

Fig. 13. 2D Normalized gain comparison plot of array with two feed networks

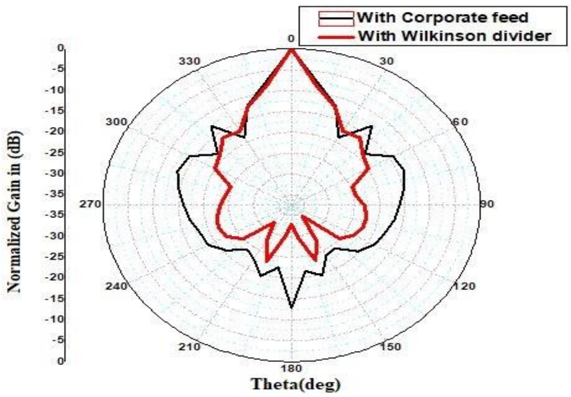

Fig. 14. Comparison of radiation pattern of array with two feed networks

Table 2. Performance comparison for 8 element array at 9.10GHz

Parameter	With Corporate feed	With Wilkinson power divider
Gain in(dBi)	12.03	12.30

Side lobe level in(dB)	-13.26	-16.48
Front to back ratio in (dB)	19.59	24.63
VSWR	1.365	1.256
Radiation efficiency (%)	59.64	56.78
3dBGain bandwidth in (MHz)	986	971
Return loss in (dB)	-15.60	-13.27

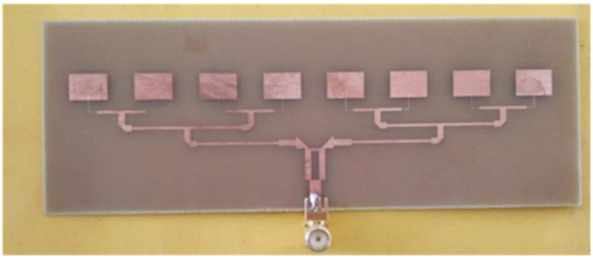

Fig. 15. 8-element array antenna with Wilkinson power divider

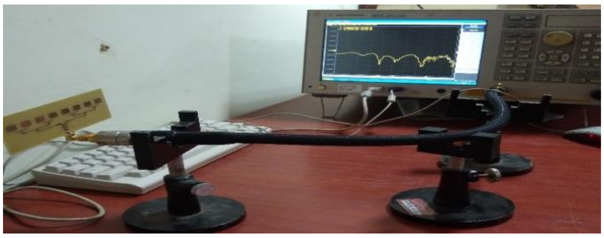

Fig. 16. Experimental setup for measurements using VNA

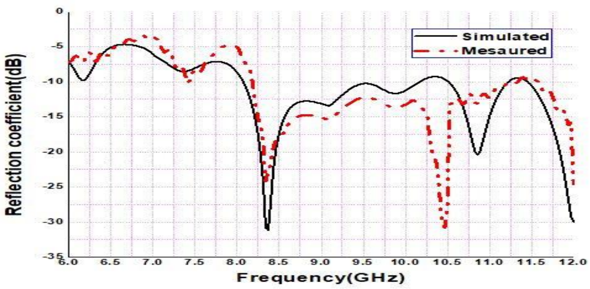

Fig. 17. S_{11} plot of the array with Wilkinson power divider

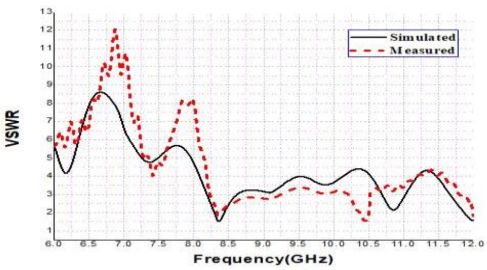

Fig. 18. VSWR plot of the array with Wilkinson power divider

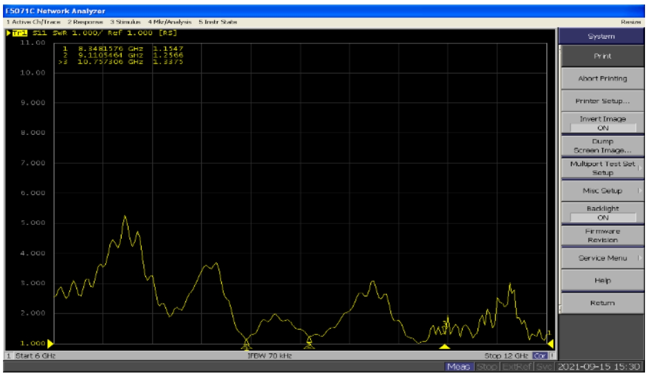

Fig. 19. Measured VSWR plot of the array with Wilkinson power divider

6. Conclusion

Design of linear microstrip antenna array with hybrid Wilkinson power divider for simultaneous side lobe reduction as well as improvement in front to back ratio is proposed in this work. From The results a 3.22dB reduction in first side lobe level and 5.04dB improvement in front to back ratio is achieved. The second and higher side lobe levels are much decreased hybrid Wilkinson power divider when compared to single corporate power divider. It is clear that the peak gain has been maintained by using same but slight decrease in radiation efficiency. This technique of hybrid power divider can be used in the efficient design of large planar antenna array suitable for X-band applications.

References

[1] Zhang Xiao, et al. "Sidelobe-Reduced and Gain-Enhanced Square Patch Antennas With Adjustable Beamwidth Under TM 03 Mode Operation." IEEE Transactions on Antennas and Propagation, vol. 66, no. 4, Apr. 2018, pp. 1704–13, https://doi.org/10.1109/TAP.2018.2806220.

[2] Manikandan, Ramamoorthy, et al. "Low Sidelobe Level CSRR Loaded Weighted Array Antenna." IEEE Transactions on Antennas and Propagation, vol. 66, no. 12, Dec. 2018, pp. 6893–905, https://doi.org/10.1109/TAP.2018.2870335.

[3] Singh, Bharati, et al. "Compact Planar Antenna Array With Tapering in Both Planes for Desired First Sidelobe Reduction." IEEE Antennas and Wireless Propagation Letters, vol. 18, no. 3, Mar. 2019, pp. 531–35, https://doi.org/10.1109/LAWP.2019.2896114.

[4] Silveira, Eduardo S., et al. "Design of Microstrip Antenna Array with Suppressed Back Lobe." Journal of Microwaves, Optoelectronics and Electromagnetic Applications, vol. 16, no. 2, Apr. 2017, pp. 460–70, https://doi.org/10.1590/2179-10742017v16i2822.

[5] Ananthi, S., and S. Dhanasekaran. “Front-to-Back Ratio Improvement of a Microstrip Patch Antenna by Using Co-Planar Rod Parasitic Elements for 1.8 GHz Wireless Applications.” 2017 International Conference on Energy, Communication, Data Analytics and Soft Computing (ICECDS), IEEE, 2017, pp. 1610–13, https://doi.org/10.1109/ICECDS.2017.8389720.

[6] Liang, Zhixi, et al. “A Broadband Dual-Polarized Antenna With Front-to-Back Ratio Enhancement Using Semicylindrical Sidewalls.” IEEE Transactions on Antennas and Propagation, vol. 66, no. 7, July 2018, pp. 3735–40, https://doi.org/10.1109/TAP.2018.2835500.

[7] Chen, Jian-Xin, and Quan Xue. “Novel 5:1 Unequal Wilkinson Power Divider Using Offset Double-Sided Parallel-Strip Lines.” IEEE Microwave and Wireless Components Letters, vol. 17, no. 3, Mar. 2007, pp. 175–77, https://doi.org/10.1109/LMWC.2006.890458.

[8] J L Li, “Novel Design of Wilkinson Power Dividers With Arbitrary Power Division Ratios”, IEEE Transactions on Industrial Electronics, vol. 58, no. 6, June 2011, pp. 2541-2546, https://doi.org/ 10.1109/TIE.2010.2066536.

[9] Stutzman, Warren L., and Gary A. Thiele. Antenna Theory and Design. 3rd ed, Wiley, 2013.

[10] Constantine A. Balanis, Antenna Theory Analysis And Design. 3rd ed, Wiley, 2005.

[11] Bhat, Bharathi, and Shiban K. Koul. Stripline-like Transmission Lines for Microwave Integrated Circuits. 1. rev. repr, Wiley, 1991.

[12] Haupt, Randy L. Antenna Arrays: A Computational Approach. Wiley, 2010.