International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Impacts of Properties of Dielectric Materials on VIAs in Printed Circuit Boards

A.Shan[1*], V. R. Prakash[2]

Submitted: 16/01/2024 **Revised**: 24/02/2024 **Accepted**: 02/03/2024

Abstract: Printed circuit boards, or PCBs, are essential parts of electronic devices because they provide the framework for connecting different electrical parts. Conductive paths called Vertical Interconnect Accesses (VIAs) link the various PCB layers and are essential for maintaining adequate power distribution and signal integrity. The performance and dependability of vias are greatly impacted by the dielectric material selection made for PCBs. The effects of parasitic capacitance, inductance, and impedance on the PCB layout are critical in high-frequency design. This study looks into the frequency domain analysis of VIAS on a PCB made of several types of dielectric materials. By investigating the insertion loss, return loss, and parasitic RLC, the impacts of various materials in the via on the PCB are examined. In this investigation, four dielectric materials are used. Ansys HFSS tool is used to run the simulations..

Keywords: *PCBs, dielectric materials, insertion loss, return loss and parasitic RLC.*

1. Introduction

Printed circuit boards, or PCBs, are crucial components in almost all electronic devices. It is critical to maintain uniform signal impedance on circuit boards [1]. For high-speed communication, different frequency bands are used, depending on the interface operating speed. When building high-frequency PCBs, one of the main considerations is the electrical characteristics of the PCB substrates. Two important electrical characteristics of dielectric materials used in the manufacture of printed circuit boards (PCBs) are the dielectric constant (Dk) and dissipation factor (Df) [2]. These characteristics are essential in defining the PCB's electrical performance, particularly with regard to signal integrity. The dielectric constant, alternatively referred to as the relative permittivity (ε_r), quantifies a response of a material to an applied electric field. The speed at which a signal propagates is affected by capacitance, which is indicated by a larger Dk. The characteristic impedance of the transmission lines on the PCB is influenced by Dk. The amount of energy lost as heat when electrical impulses are sent through a medium is measured by the dissipation factor, sometimes referred to as the loss tangent. Better signal integrity and less energy loss are indicated by a lower Df. Df values for low-loss materials intended for high-frequency applications can range from 0.002 to 0.015. Lower Dk and Df materials are frequently chosen for high-frequency systems in order to reduce signal distortion and loss.

Using materials with a high Dk or mismatched dielectric characteristics can have a substantial impact on signal attenuation in radio frequency (RF) or high-frequency circuits [3][26]. The characteristic impedance of transmission lines and the speed at which signals propagate are both greatly influenced by a material's dielectric constant. Signal attenuation and other unwanted effects may result from a transition between materials with varying Dk values. This attenuation may limit the highest frequency and distance that signals can travel without experiencing significant loss. A dielectric material with the appropriate Dk and Df values should be selected based on the specific requirements of the PCB design and the intended use. Low-speed digital PCBs might not be as sensitive to low Dk and low Df materials, but high-frequency and RF PCBs might require them to preserve signal integrity.

The intrinsic resistance (R), inductance (L), and capacitance (C) of components and traces are known as RLC parasitics, and they can have a significant impact on the behaviour of signals on printed circuit boards (PCBs) [4][25]. Numerous detrimental effects on rise time, signal strength, signal integrity, and overall performance can be caused by these parasitic components [5]. The resistance of the traces and other parts of the PCB may attenuate or dampen the signal as it travels through it. This could result in lower signal voltage amplitudes at the receiving end, which could lower the overall signal integrity. Component and trace length inductance can cause delays in signals. High-inductance traces can affect transmission timing because they slow down the propagation of signals. In high-frequency applications, this delay can result in timing skew and other timing-related issues. Particularly at high switching frequencies, parasitic capacitance in digital signals can result in ringing and overshoot. Because capacitance can produce a resonant circuit with the inductance, it can cause signal overshoot and oscillations. [27] The RLC parasitics have the ability to create resonant circuits at specific frequencies, which may cause unexpected signal behaviour or even signal loss. Impedance mismatches may result from the parasitics RLC along transmission lines. As a result, signal reflections at discontinuities may cause signal distortion and poor-quality issues. Reducing these effects requires accurate impedance matching.

This paper is organized as follows. Section II outlines the related literature. Section III explains the analysis of losses and parasitic RLC for four dielectric materials. The simulation results are discussed in Section IV with concluding remarks in section V.

[1]*Department of ECE, Hindustan Institute of Technology and Science, Chennai, Tamil Nadu India, Email: shan.ar4@gmail.com**
[2]*Department of ECE, Hindustan Institute of Technology and Science, Chennai, Tamil Nadu India, Email: vrprakash@hindustanuniv.ac.in*

2. Related Works

The signal propagation in the PCB can be enhanced by selecting an impedance that increases the matching between a line and a VIA, as demonstrated by Mallikarjun et al. [6]. Pan et al. proved that a differential VIA structure necessitates the simultaneous optimisation of all associated parameters [7]. The effects of different route design factors on signal integrity are thoroughly examined in the literature [8]. Asif et al. demonstrated that while every geometrical parameter has an impact on differential VIA performance, those impacts varied [9]. In literature [10], the parameters of the fencing mechanism in PCB boards have been plotted to limit coupling at the board level in a multilayer PCB with a high data rate. In contrast, it would leave tracks along the top side of the ground plane in real-world settings. Losses resulting from impedance mismatch, crosstalk, and EMI are the three signal integrity problems that multilayer PCB transmission lines can experience. The length of the cable at the curve contributes to signal reflection and erratic impedance [11]. The "quick approach" has been used to conduct time domain analysis [12]. It uses complete factor optimization and provides a rapid turnaround period by anticipating the factor of too-capacitive or inductive performance. Uneven power dividers are what lead to the impedance match between transmission lines and stubs [13, 14]. However, its applications require high-impedance transmission lines exclusively. The electromagnetic simulation program HFSS has been used to calculate the power transparency and signal integrity debate in three dimensions [15].

By showing that proper positioning can yield better outcomes than the random placement of more ground VIAs, Chen et al. [16] demonstrated how symmetrical structures should be used in conjunction with the optimisation of ground VIA placements. The impedance discontinuity is one of the key sources in the interconnection channel that has been improved. Via spacing is described in [17] explains that horizontal spacing is used for high voltage and vertical spacing for low voltage. The discussion concluded that the ideal PCB must supply the proper thermal impedance and carry current. Guz et al. addressed the trade-offs necessary to create dependable and functioning digital PCBs as well as the practical difficulties of powering complicated multilayer PCBs from high-energy sources [18]. Barzdenas and Vasjanov [19] explained how to track PCB discontinuities to provide the correct level of impedance. The cut-out correction in the reference plane is implemented by modifying capacitance and inductance per unit length. According to Bell et al., the experimental properties of stiff flex PCB are influenced by the mode shape, nonlinear features, and frequency characteristics [20]. In literature [21], The authors enhanced the impedance by combining channel simulations with time-domain impedance waveforms [21]. The main contributions of this work are as follows. There are four dielectric materials such as 370HR_106PP, IS410, EM_827_PP_2116 and FR5 are considered for investigations of insertion loss, return loss and parasitic RLC. The impacts of these parameters are discussed briefly.

3. Effects of Insertion Loss, Return Loss and Parasitic RLC

The primary factors influencing power and signal integrity, as well as the effectiveness of vias in printed circuit boards, are as follows.

a) Insertion loss

High insertion loss dielectric materials have the ability to attenuate high-frequency signals when they go through vias. Higher data rates cause this attenuation to become more noticeable and can cause signal degradation, which can cause problems like data mistakes and a shorter communication range. Insertion loss is measured as a variation in signal power at the time the component is inserted, and it is commonly reported in decibels (dB). Filters, amplifiers, and connectors that have low insertion loss suggest that there is little loss of signal power during transmission. It is given by,

$$\text{Insertion loss} = -10 \cdot \log_{10}\left(\frac{P_o}{P_i}\right) \quad (1)$$

where, P_o is the output power and P_i is the input power.

b) Return loss

The reflected power at the discontinuity or impedance mismatch point in a transmission line or device is measured as return loss. The ratio of reflected power to incident power is used to compute return loss, which is also measured in decibels (dB). Better impedance matching and fewer signal reflections are indicated by higher return loss values, which are essential for reducing signal distortion and guaranteeing effective power transfer. The return loss is expresses as,

$$\text{Return loss} = -10 \cdot \log_{10}\left(\frac{P_{ref}}{P_{inc}}\right) \quad (2)$$

where, P_{ref} and P_{inc} are the reflected power and incident power respectively.

A low return loss might provide greater signal reflections at the via, resulting in signal distortions. Signal deterioration may be exacerbated by these reflections, particularly in high-frequency and high-speed digital applications. In this analysis, there are four different materials are used as shown in Table 1.

Table 1. Types of materials and properties

Materials	Dielectric constant (Dk)	Dissipation factor (Df)
370HR_106PP	3.54	0.031
IS410	3.87	0.023
EM_827_PP_2116	4.05	0.0205
FR5	4.2	0.014

Figure 1 shows the insertion loss (IL) and return loss (RL) of four dielectric materials at 35 GHz. For 370HR_106PP material, the insertion loss and return loss is about -1.92 and 8.17 respectively shown in in Figure 1(a). For IS410, IL is about -1.79 and RL is 7.88 shown in Figure 1(b). For EM_827_PP_2116 material, IL is about -1.76 and RL is 7.77 shown in Figure 1(c). For FR5 material, IL is about -1.46 and RL is 7.76 shown in Figure 1(d). Table 2 summarizes the simulation results of IL and RL for dielectric materials used in this study.

Table 2. IL and RL for four dielectric materials

Materials	Insertion Loss @ 35GHz	Return Loss @ 35GHz
370HR_106PP	-1.9237dB	-8.1744 dB
IS410	-1.7914 dB	-7.8795 dB
EM_827_PP_2116	-1.7606 dB	-7.7709 dB
FR5	-1.4643 dB	-7.7633 dB

c) Parasitic RLC

VIAs (interconnects) on PCBs can be severely impacted by parasitic RLC components in dielectric materials, especially in high-frequency and high-speed applications. Comprehending the

effects of these parasitics is essential for creating PCBs with ideal power distribution and signal integrity. In this work, parasitic RLC is calculated at 200 MHz and 400 MHz frequencies for four dielectric materials as shown in Figure 2. The obtained parasitic RLC components for four materials are as follows.

(i) For 370HR_106PP material, at 200 MHz, the resistance (R) is 46.0899 mΩ, inductance (L) is about 2.2147 nH and capacitance (C) is 0.60739 pF. At 400 MHz, the resistance (R) is 69.38 mΩ, inductance (L) is about 2.2145 nH and capacitance (C) is 0.59845 pF.

(ii) For IS410 material, the resistance (R) is 47.66 mΩ, inductance (L) is about 2.2091 nH and capacitance (C) is 0.6584 pF at frequency of 200 MHz. The resistance (R) is 66.71 mΩ, inductance (L) is about 2.2138 nH and capacitance (C) is 0.6440 pF at frequency of 400 MHz.

(iii) For EM_827_PP_2116 material, the resistance (R) is 43.63 mΩ, inductance (L) is about 2.2012 nH and capacitance (C) is 0.6868 pF at frequency of 200 MHz. The resistance (R) is 67.25 mΩ, inductance (L) is about 2.2083 nH and capacitance (C) is 0.6735 pF at frequency of 400 MHz.

(iv) For FR5 material, the resistance (R) is 43.13 mΩ, inductance (L) is about 2.2065 nH and capacitance (C) is 0.6895 pF at frequency of 200 MHz. The resistance (R) is 69.35 mΩ, inductance (L) is about 2.2050 nH and capacitance (C) is 0.6862 pF at frequency of 400 MHz.

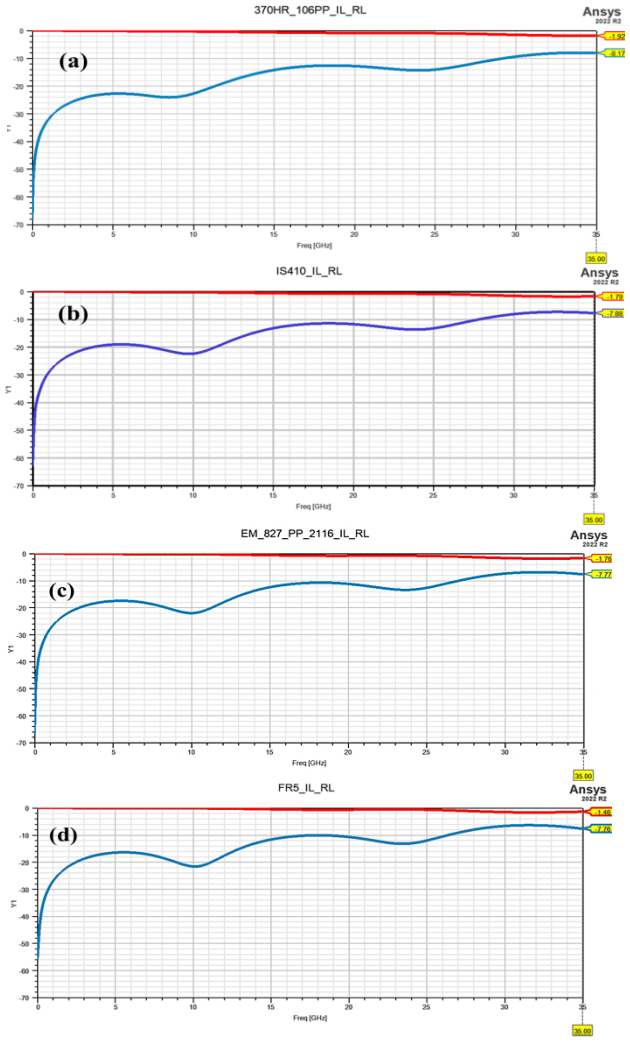

Fig. 1. Insertion loss (red) and return loss (blue) for four materials used.

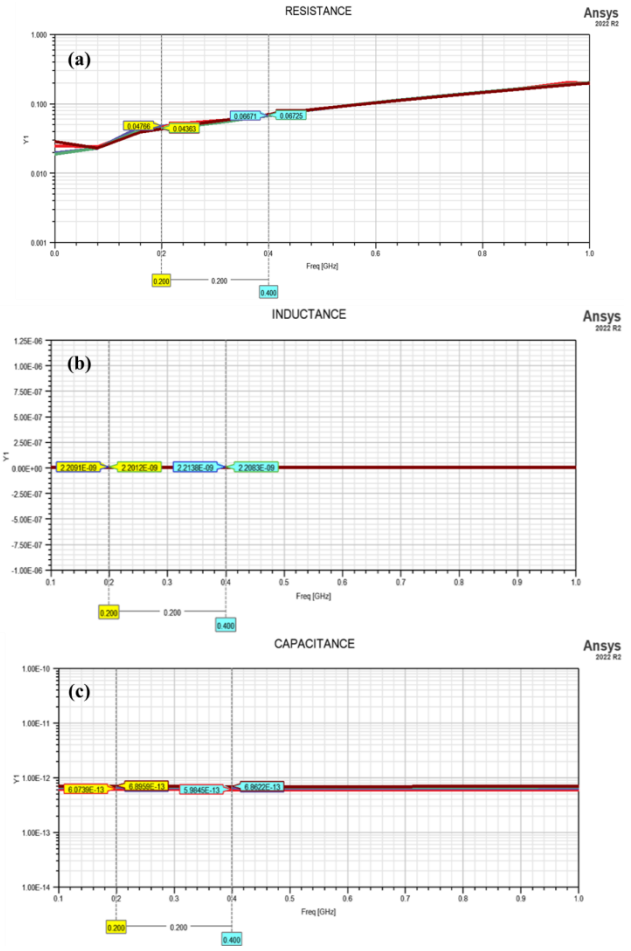

Fig. 2. Simulation results of parasitic RLC for four dielectric materials 370HR_106PP (red), IS410 (blue), EM_827_PP_2116 (green) and FR5 (brown).

Table 3. A summary of the parasitic RLC for four dielectric materials.

Materials	@200MHz		
	Inductance (nH)	Resistance (mΩ)	Capacitance (pF)
370HR_106PP	2.2147	46.09	0.6073
IS410	2.2091	47.66	0.6584
EM_827_PP_2116	2.2012	43.63	0.6868
FR5	2.2065	43.13	0.6895
Materials	**@400MHz**		
	Inductance (nH)	**Resistance (mΩ)**	**Capacitance (pF)**
370HR_106PP	2.2145	69.38	0.5984
IS410	2.2138	66.71	0.6440
EM_827_PP_2116	2.2083	67.25	0.6735
FR5	2.2050	69.35	0.6862

4. Discussion

Ansys High Frequency Structure Simulator (HFSS), a full-wave electromagnetic simulation programme, was used to simulate each design in this investigation. The analysis shows that a material with a high dissipation factor (Df) has large signal losses, while a material with a low Df has little losses. While materials with high dielectric constants slow down signal transmission, those with low dielectric constants (Dk) allow for speedier signal propagation. Signal integrity is an aspect to consider when analysing the signal in high-speed circuits. The

fast speed of the frequency domain analysis allows for the immediate visualisation and identification of a signal's essential electrical quality components. For every approach that is given, a PCB's VIAs are analysed. The results can be witnessed in each of the four simulation settings.

In high-frequency PCB designs, dielectric materials with lower Dk values—particularly those in the 3.5 range—are typically thought to be superior in terms of return loss. For insertion loss, the materials with a low Df are preferable. Reduced Df values minimise energy loss during signal transmission through the dielectric medium, which improves signal integrity. More energy loss and insertion loss are indicated by a greater Df, particularly in high-frequency applications.

The signal loss will decrease as resistance decreases. High Dk materials have high capacitance, while low Dk materials have high inductance. Dielectric materials on the PCB affect crosstalk between adjacent traces. Higher DK materials may result in increased crosstalk and stronger capacitive coupling. Selecting a low DK material is essential if we want to go for a high-speed signal. Transmission lines' characteristic impedance is strictly controlled by their dielectric properties. The impedance of the traces must match the design criteria in order for the signal to remain intact. Factors like layer thickness and dielectric constant must be taken into account in order to obtain the right impedance. An electronic device will last longer if the right dielectric material is chosen since it will reduce losses and improve performance and durability.

From the results, it is observed that 370HR_106PP and FR5 typically have higher Dk values than IS410 and EM_827_PP_2116. In general, 370HR_106PP and FR5 show higher Df values than IS410 and EM_827_PP_2116. Because of their reputation for having smaller insertion losses, IS410 and EM_827_PP_2116 are appropriate for high-frequency applications where reducing signal attenuation is essential. FR5 and 370HR_106PP both exhibit moderate insertion loss characteristics. Given their low Df values, IS410 and EM_827_PP_2116 should offer good return loss performance. Returned loss for 370HR_106PP and FR5 is contingent upon particular dielectric characteristics and product compositions.

5. Conclusion

This study investigates the effects on PCB VIAs of dielectric materials' insertion loss, return loss, and parasitic RLC. Four dielectric materials, including FR5, IS410, EM_827_PP_2116, and 370HR_106PP, were selected for the analysis. While the low insertion loss characteristics of IS410 and EM_827_PP_2116 are well-known, the performance of FR5 and 370HR_106PP is dependent upon certain dielectric qualities and product formulations. Given their low Df values, IS410 and EM_827_PP_2116 should offer good return loss performance. The decision should be based on the application's particular needs and limitations.

References

[1] T. Huesgen, “Printed circuit board embedded power semiconductors: A technology review,” Power Electronic Devices and Components, vol. 3, 2022.

[2] D. Brooks and J. Adam, PCB Design Guide to Via and Trace Currents and Temperatures, Artech, 2021.

[3] W. Jillek, W. Yung, “Embedded components in printed circuit boards: A processing technology review,” The International Journal of Advanced Manufacturing Technology, 25, pp. 350–360, 2005.

[4] A. Shan and V. R. Prakash, “Certain Investigations on Eye Diagram Observation for Different Frequencies in Printed Circuit Board,” Mobile Computing and Sustainable Informatics. Lecture Notes on Data Engineering and Communications Technologies, vol. 166, 2023. https://doi.org/10.1007/978-981-99-0835-6_44

[5] J. Fan et al., “A. Signal Integrity Design for High-Speed Digital Circuits: Progress and Directions,” IEEE Trans. Electromagn. Compat. 2010, 52, 392–400.

[6] M. Vasa, et al., “Demystifying Via Impedance Optimization for High-Speed Channels,” In Proceedings of the 5th International Conference on ElectroMagnetic Interference and Compatibility (INCEMIC), Bengaluru, India, 13–16 November 2018.

[7] S. Pan and J. Fan, "Equivalent mixed-mode characteristic impedances for differential signal vias," 2009 IEEE International Symposium on Electromagnetic Compatibility, Austin, TX, USA, 2009, pp. 74-79, doi: 10.1109/ISEMC.2009.5284632.

[8] Chang, R. W. Y., See, K. Y., & Chua, E. K. (2007, December). Comprehensive analysis of the impact of via design on high-speed signal integrity. In 2007 9th Electronics Packaging Technology Conference (pp. 262-266). IEEE.

[9] Asif, A. Design of Experiment Methods in High-Speed Signal Via Transition in Printed Circuit Board. Int. J. Eng. Technol. Innov. 13, 2019.

[10] Chang, R. W. Y., See, K. Y., & Chua, E. K. (2007, December). Comprehensive analysis of the impact of via design on high-speed signal integrity. In 2007 9th Electronics Packaging Technology Conference (pp. 262-266). IEEE.

[11] Tortorich, R. P., Morell, W., Reiner, E., Bouillon, W., & Choi, J. W. (2021). A Study on the Radiated Susceptibility of Printed Circuit Boards and the Effects of Via Fencing. Electronics, 10(5), 539.

[12] Wu, Q., Li, Y., Liu, J., & Jiao, Y. (2019, March). High Speed Muti-board Signal Integrity Simulation and Implementation. In 2019 IEEE International Conference on Artificial Intelligence and Computer Applications (ICAICA) (pp. 444-447). IEEE.

[13] Vardapetyan, A., & Ong, C. J. (2020, October). Via design optimization for high-speed differential interconnects on circuit boards. In 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS) (pp. 1-3). IEEE.

[14] Xu, G., Eleftheriades, G. V., & Hum, S. V. (2021). Analysis and design of general printed circuit board metagratings with an equivalent circuit model approach. IEEE Transactions on Antennas and Propagation, 69(8), 4657-4669.

[15] Yoon, Y. C., & Kim, Y. (2021). Unequal Power Dividers Using Uniform Impedance Transmission Lines with Stubs. Journal of Electromagnetic Engineering and Science, 21(1), 44-50.

[16] S. Chen, C. Chen, C. -L. Liao, J. Chen, T. -L. Wu and B. Mutnury, "Via optimization for next generation speeds," 2017 IEEE 26th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2017, pp. 1-3, doi: 10.1109/EPEPS.2017.8329730.

[17] Yang, Z., Gao, Y., Li, S., Sun, C., & Zhao, Y. (2021, October). Research on Signal Integrity in High-Speed Interconnection Channel Based on SIwave. In 2021 IEEE 3rd International Conference on Circuits and Systems (ICCS) (pp. 78-82). IEEE.

[18] M. Guz, "Practical Considerations for Design and Layout of High-Power Digital PCBs: Reliably Powering Complex Multilayer Digital

Printed Circuit Boards," in IEEE Power Electronics Magazine, vol. 8, no. 2, pp. 53-59, June 2021, doi: 10.1109/MPEL.2021.3075757.

[19] Barzdenas, V., &Vasjanov, A. (2022). A Method of Optimizing Characteristic Impedance Compensation Using Cut-Outs in High-Density PCB Designs. Sensors, 22(3), 964.

[20] Bell, J., Redmond, L., Carpenter, K., & de la Croix, J. P. (2022). Experimental dynamic characterization of rigid-flex PCB systems. Experimental Techniques, 1-15.

[21] A. Vardapetyan and C. -J. Ong, "Via Design Optimization for High-Speed Differential Interconnects on Circuit Boards," 2020 IEEE 29th Conference on Electrical Performance of Electronic Packaging and Systems (EPEPS), San Jose, CA, USA, 2020, pp. 1-3, doi: 10.1109/EPEPS48591.2020.9231314.

[22] Abd, Shamis N., Mohammad Alsajri, and Hind Raad Ibraheem. "Rao-SVM machine learning algorithm for intrusion detection system." Iraqi Journal For Computer Science and Mathematics 1.1 (2020): 23-27.

[23] Salih, Hayder Sabah, Mohanad Ghazi, and Mohammad Aljanabi. "Implementing an Automated Inventory Management System for Small and Medium-sized Enterprises." Iraqi Journal For Computer Science and Mathematics 4.2 (2023): 238-244.

[24] Al-Janabi, Mohammed, and Mohd Arfian Ismail. "Improved intrusion detection algorithm based on TLBO and GA algorithms." Int. Arab J. Inf. Technol. 18.2 (2021): 170-179.

[25] A. K. Sahu, V. K. Chandra and G. R. Sinha, "High level computation technique for characterization of sigma-delta a/d converter," 2017 International conference on Microelectronic Devices, Circuits and Systems (ICMDCS), Vellore, India, 2017, pp. 1-4, doi: 10.1109/ICMDCS.2017.8211601.

[26] Soma, S., Gowre, S.K.C., Sonth, M.V. et al. Design and simulation of reconfigurable optical logic gates for integrated optical circuits. Opt Quant Electron 55, 340 (2023). https://doi.org/10.1007/s11082-022-04532-8

[27] Sonth, M.V., Gowre, S., Biradar, N., Gadgay, B. (2020). Design and Simulation of AND-OR-INVERT Logic for Photonic Integrated Circuits. In: Mandal, J., Bhattacharya, K., Majumdar, I., Mandal, S. (eds) Information, Photonics and Communication. Lecture Notes in Networks and Systems, vol 79. Springer, Singapore. https://doi.org/10.1007/978-981-32-9453-0_6