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A Novel Zipper Logic Based Hybrid 1-Bit Full Adder Circuit Design

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Abstract: Zipper logic is a design that integrates many logic types or approaches to create an efficient and optimal circuit. A 1-bit Full Adder (FA) is a basic building block in digital circuits that adds two 1-bit binary inputs (A and B) plus a Carry Input (Cin) to create a sum output (S) and a Carry Output (Cout). This study examined the concept of a zipper logic-based hybrid 1-bit FA circuit design, which pertains to a particular method of designing a digital circuit that performs the addition operation on two 1-bit binary integers (bits). The performance parameters of the hybrid circuit are assessed and compared to standard 1-bit FA designs, revealing considerable improvements in latency and energy usage. The suggested FA cell's performance has been analyzed using a Cadence simulator at the 16 nm production node, where it was compared to that of existing FAs throughout a supply voltage spectrum of 0.4 to 1.0 V. When compared to the other adder, the suggested adder improved Average Power Consumption (ADP) by 48.9% and Power Delay Product (PDP) by 66.7% when conducting at 0.8V.

Keywords: *Complementary Metal-Oxide-Semiconductor (CMOS) Logic, Hybrid Circuit Design, Performance Evaluation., Zipper Logic, 1-bit Full Adder*

1. Introduction

Arithmetic circuits are crucial to the successful execution of the specialized algorithms used by Application Specific Integrated Circuits and Digital Signal Processing (DSPs), such as correlation, convolution, and digital filtering, and hence to their overall performance. In general terms, integrated circuits' efficiency depends on the quality of their execution of arithmetic operators in the cell library made available to the designer during the synthesis process. Due to transistors ' ever-increasing complexity and density, energy efficiency and processing speed are now essential in integrated circuits. To keep up with the needs of the expanding business sector, several CMOS Logic variants have been produced and are always being improved upon. Increasing circuit latency and degrading the driving performance of specified cells in particular logic styles are unavoidable consequences of reducing power consumption in ultra-deep submicron technology [1].

An FA performs various mathematical operations, including addition, subtraction, multiplication, and accumulation, and is a crucial part of microprocessors and other sophisticated circuits. As a result, it stands to reason that the FA performance would affect the whole system [2, 3]. Thus, there has been significant study into developing efficient 1-bit FA cells at fast speeds with low power consumption [4]. A FA takes in three inputs: A, B, and Cin, where Cin is the carry input from the preceding block and produces two results, the sum and the Cout [5]. The operation of a 1-bit FA could be expressed as a Boolean equation which is,

$$Sum = A_{\oplus}B_{\oplus}Cin \dots\dots\dots\dots\dots\dots\dots \quad (1)$$

$$Cout = A.B + A.Cin + B.Cin \dots\dots\dots\dots (2)$$

Several methods have been used to create an FA circuit that uses few transistors, consumes less energy, and operates at higher speeds [6]. The number of transistors in Conventional CMOS logic causes it to use more space and energy than alternative implementations based on pseudo-N-channel metal-oxide semiconductor (NMOS) or transistor technology [7]. In contrast, the dynamic logic style is an alternative one that employs a series of pre-charge and conditional evaluation phases regulated by the clock to implement complicated logic functions, resulting in decreased latency and higher speed. In this method, N transistors are utilized to create a pull-up (PMOS) and pull-down (NMOS) network, with an extra two transistors used to turn the circuit on and off at the appropriate times (during evaluation and standby mode) using a clock signal [8].

1.1. Advancing 1-Bit Full Adder Circuitry

The Full Adder, also known as the FA, is the most essential part of an arithmetic-logic unit (ALU). The relevance of this extends to a variety of logical and arithmetic operations, including multiplication, addition, subtraction, and division. The action of addition is particularly significant in the design of virtual logic architecture. The speed of the central processing unit is used as an innovation metric for FAs [9]. The performance of the overall adder architecture determines the level of accuracy and speed at which digital systems can function. Utilizing strategies such as Pass-Transistor Logic (PTL) and Pseudo NMOS may help

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optimize the transistor count for logic operations, even though this results in an increase in the amount of power used.

The sum (S) and the carry outputs (Cout) of a simple FA are derived from a total of three inputs. Gates that operate according to the XOR, AND, and OR logic operations are required to build this adder's logic circuit. While AND/OR gates control carry logic, XOR gates are responsible for handling particular logic. A block diagram of a 1-bit FA may be shown in Fig 1. This design processes the inputs A, B, and Cin to produce the outputs S and Cout. A FA's truth table is shown in Table 1, which contains its contents. Hybrid design innovations have the potential to advance 1-bit FA circuitry by bringing together different logic approaches in a harmonious way, hence improving the computational performance of ALUs and digital systems [10].

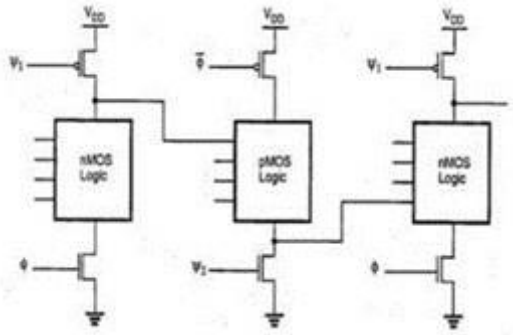

Fig 1 Circuit Diagram zipper logic circuit [11]

Table 1. The Truth Table of FA [12]

Inputs			Outputs	
A	**B**	**Cin**	**Sum**	**C_{out}**
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

1.2. CMOS Login in 1-Bit Full Adder Design

A 1-bit FA circuit relies heavily on Complementary Metal-Oxide-Semiconductor (CMOS) logic. The adder relies on this logic design, which combines n-type and p-type transistors. One-bit FA uses CMOS circuitry because it allows for efficient signal processing while computing the sum and carry outputs of three input bits [13].

To function, CMOS logic makes use of the different ways in which complementary transistor pairs conduct electricity. When a designated input voltage level is provided, the n-type or p-type transistor becomes conductive, allowing current to pass through the circuit. To accomplish its arithmetic operations, the 1-bit FA combines these two kinds of transistors in a variety of combinations, including NAND, NOR, and XOR gates [14]. The 1-bit FA is designed using CMOS circuitry that balances efficiency with speed and precision in calculation. To strike this equilibrium, one must give some thought to transistor size, voltage, and circuit architecture. The 1-bit FA circuit can analyze input signals and provide precise sum and carry outputs thanks to the strategic placement and optimization of CMOS components. In conclusion, CMOS logic is an essential component in the development of a 1-bit FA circuit [15]. In digital logic applications, its ability to regulate current flow between complementary transistor pairs is crucial for performing accurate arithmetic calculations.

The motive of this study is to create an innovative and efficient 1-bit FA circuit that integrates Zipper logic concepts with other hybrid design strategies. The major objective is to decrease power consumption, propagation delay, and circuit size while retaining good performance and reliability. The design should be based on the Zipper logic idea, which employs both pass-transistor and complementary CMOS logic types, and it should include appropriate optimizations and innovations to achieve enhanced overall performance compared to typical FA designs. The proposed circuit should be thoroughly simulated, validated, and compared with current other FA designs to demonstrate its power efficiency, speed, and area utilization superiority.

- To develop a novel 1-bit FA circuit using a zipper logic-based hybrid approach.
- To analyze and compare the power efficiency and speed of the proposed FA circuit with those of existing designs.
- Investigate the scalability and applicability of the zipper logic-based hybrid approach for larger multi-bit adders.
- Evaluate the robustness and reliability of the proposed circuit under several operating conditions and technology variations.

The study follows the following structure: Section 2, provides a literature review on zipper logic-based hybrid 1-bit FA circuit design. The study methodology and methods are introduced in Section 3, and the recommended method is proven. The anticipated findings are presented in Section 4. The paper further then comes to a conclusive verdict and suggests areas that need more research in section 5.

2. Review of Literature

This section defines the previous studies of several authors built on a novel Zipper logic-based hybrid 1-bit FA circuit design.

Ghorbani et al., (2022) [16] presented a new energy-efficient FA circuit through the utilization of Carbon Nanotube Field-Effect Transistors (CNFET) technology by fusing the dynamic logic approach with the low-power Gate Diffusion Input (GDI) method. The study effectively built essential logic components such as XOR and XNOR gates, leading to the development of a complete full-swing, FA cell based on CNFET. The simulation results showed that the new FA circuit design significantly improved upon important circuit factors such as power delay product (PDP), consumption of power or energy, and latency.

Zareei et al. (2021) [17] introduced novel ferroelectric (FA) cells utilizing carbon nanotube field-effect transistors (CNFETs) and capacitive threshold logic (CTL) technology. The study employed application- and transistor-level simulations to evaluate these cells. The cells in Cadence undergo an image processing procedure to compute the Peak signal-to-noise ratio (PSNR). HSPICE was used to provide hardware assessment parameters such as power consumption, latency, and power-delay product (PDP). The paper examined noise assessment by the utilization of average noise threshold energy (ANTE) and noise immunity curve (NIC), which ensures a suitable equilibrium between application and hardware metrics.

Rafiee et al., (2021) [18] presented a low-power 1-bit FA cell based on transmission gate (TG) technology. The goal of this novel strategy was to design a dedicated module capable of producing a Carry output in full swing. The TG-based FA had strong driving capabilities for the Sum and Carry outputs, making it applicable to multistage architectures such as ripple-carry adders (RCAs), compressors, and multipliers. This FA was remarkable since it only requires a 60.02 m2 die space, used 10.829 W of power on average, had a latency of 3.1954 ns, and a PDP of 34.603 fJ. These results established the TG-based FA as a promising candidate for use in integrated circuits (ICs).

Hussain et al., (2021) [19] introduced a new complete adder circuit layout for use in VLSI-based computational arithmetic. This architecture used GDI methods and input-switching activity patterns. The design process of the adder was carried out in two stages: the first stage consisted of the implementation of an XOR-XNOR circuit, and the second stage was responsible for supplying the required outputs. Minimizing transistor switching activities by using switching activity patterns and GDI approaches at each level improved delay, power efficiency, and computational complexity. The proposed adder showed outstanding gains, with speed increases of at least 72.86% and energy savings of at least 66.67%. Extensive performance evaluations were carried out at the 32 nm CNFET nodes and 32 nm CMOS with encouraging results at both nodes.

Shewale S. et al., (2021) [20] provided a complete analysis of FA circuits using Complementary MOSFETs (CMOS). The authors have taken a different strategy, using complete adder circuits in a hybrid design. The construction of an FA circuit was a prerequisite for many other digital system components. Many electronic devices rely on it, including Microcontrollers, Microprocessors, and DSPs. The suggested FA cell was more space-efficient and uses less power. The increasing need for computer systems that were both energy-efficient and high-performing have led to a recent rise in research interest in this field. They wanted to do this by designing FA circuits in many technologies and comparing their power capacities. The authors have realized the whole adder circuit utilizing an NMOS/PMOS hybrid construction.

Parameshwara M.C. et al., (2021) [21] developed an innovative 1-bit FA using 22 transistors (22T) for use in VLSI systems. The suggested FA is based on hybrid logic, which combines the GDI approach, TGs, and Static Complementary Metal-Oxide-Semiconductor (SCMOS) logic. The simulation findings demonstrate that for varying levels of Vdd, only the suggested FA and the other two described can function in 64b Ripple Carry Adder (RCA) without resorting to intermediate buffers. Further, the recommended FA outperforms the other two FAs regarding power, latency, and Transistor Count (TC).

Hasan M. et al., (2021) [22] presented the combined three logic methods, traditional CMOS, Pass Transistors (PTs), and TGs to provide a fast-speed hybrid FA based on an XOR-XNOR circuit. The FA circuit design have been compared and validated against ten state-of-the-art FAs to determine its efficacy. The measurements of the FA's performance as a 1-bit adder cell and wide word length adder indicated good results. Therefore, the proposed hybrid FA could alternatively replace the traditional FAs employed in modern microprocessors' digital arithmetic blocks.

Keerthana et al., (2020) [23] introduced a hybrid design that makes use of many logic systems, each of which performs a specific task within the overall architecture. Importantly, their FA concept requires just a single bit of data and has been thoroughly tested on a 22-nm Complementary Metal-Oxide Semiconductor (CMOS) hybrid platform. The low-latency and low-power properties of the architecture have been verified through simulations. With a 0.8 V supply and 22 nm technology, the study presented a latency of less than 7.0415 ps and an average power usage of less than 1.1055 W. Overall, this form of adder was a huge improvement over earlier complete adder designs in terms of power economy, speed, and space.

Hasan et al., (2020) [24] presented a high-speed hybrid FA cell that combined GDI with conventional CCMOS logic. After running simulations on a 45 nm CMOS technology used Cadence CAD tools, the design beat 10 different FAs in terms of speed and PDP. Both the suggested design and five current designs fared well when their bit depth was

doubled to 32, but the proposed design shone in more complex cascaded circuits, displaying improved performance metrics.

Sadeghi A. et al., (2020) [25] found a novel technique for designing circuits called Pseudo-Dynamic Logic (PDL), which has benefits like both static and dynamic cells. A brand-new 18-transistor FA cell is used to calculate the PDL's worth. After the layout was complete, simulation was done, and digital images were added to assess how the cell would function in its intended situation. Cell performance in image processing was measured utilizing the Structural Similarity Index Metric (SSIM), Mean Square Error (MSE), and PSNR. The suggested PDL-based FA cell outperforms dynamic and static circuits, proving its efficacy. Table 2 presents a comparative analysis of reviewed literature in terms of techniques and outcomes.

Table 2 Comparative Analysis of Reviewed Literature

Authors	Technique	Outcomes
Ghorbani et al., (2022) [16]	CNFET GDI	The results of the simulations showed that the proposed FA significantly improved power consumption, latency, and PDP.
Zareei et al., (2021) [17]	CNFET CTL	Results from computer simulations verify the superiority of the suggested cells compared to competing solutions.
Rafiee et al., (2021) [18]	TG-based FA	The proposed FA only required a 60.02 m2 die space, uses 10.829 W of power on average, has a latency of 3.1954 ns, and a PDP of 34.603 fJ.
Hussain et al., (2021) [19]	VLSI CNFET CMOS	The proposed adder showed outstanding gains, with speed increases of at least 72.86% and energy savings of at least 66.67%.
Shewale S. et al., (2021) [20]	NMOS/PMOS	The suggested FA cell was more space-efficient and uses less power.
Parameshwara M.C. et al., (2021) [21]	GDI TG SCMOS	The recommended FA outperforms the other two FAs regarding power, latency, and TC.
Hasan M. et al., (2021) [22]	CMOS TG PT	The measurements of the FA's performance as a 1-bit adder cell and wide word length adder indicated good results.
Keerthana et al., (2020) [23]	CMOS	The study presented a latency of less than 7.0415 ps and an average power usage of less than 1.1055 W.
Hasan et al., (2020) [24]	GDI CCMOS	The proposed design shone in more complex cascaded circuits, displaying improved performance metrics.
Sadeghi A. et al., (2020) [25]	PDL	The suggested PDL-based FA cell outperforms dynamic and static circuits, proving its efficacy.

3. Material and Methods

A Zipper Logic-based Hybrid 1-bit FA Circuit involves several steps, including designing the individual components, arranging them on a chip, and connecting them properly [26]. The process, along with some considerations.

3.1. Equations

Design Tools: Electronic Design Automation (EDA) tools for schematic capture, layout design, and simulation. Popular tools include Cadence Virtuoso, Synopsys Design Compiler, and Mentor Graphics tools.

Technology Library: a library containing the standard cells, transistors, and other components available in the target technology node.

Design Rules and Guidelines: Familiarize with the design rules and guidelines provided by the foundry or technology provider. These rules ensure that the design can be fabricated correctly.

3.2. Method Layout

Schematic Design: Create a Zipper Logic-based hybrid 1-bit FA circuit schematic utilizing the EDA tool's schematic capture interface. Use this schematic to represent the circuit's logical behavior.

Component Selection: Choose appropriate standard cells from the technology library for each component in the schematic, such as NAND, NOR XOR, XNOR gates, multiplexers, transmission gates, etc.

Layout Design: Floor planning: Decide on the overall chip size and allocate areas for different circuit sections, such as input/output pads, core logic, and power distribution.

Placement: Place the selected standard cells on the chip according to the circuit's schematic. Consider factors like signal connectivity, proximity, and optimal placement for minimizing wire lengths.

Routing: Connect the placed cells using metal tracks and vias to establish the required connections. Follow the design rules to ensure proper spacing, width, and alignment of metal traces.

Power Distribution: Design a network to ensure all components receive proper power and ground connections.

Clock Distribution: If the design uses a clock signal, plan and route the clock distribution network to ensure synchronization.

DRC and LVS Checks: Design Rule Checking (DRC) and Layout Versus Schematic (LVS) checks to ensure the layout adheres to the foundry's design rules and matches the original schematic.

Extraction and Simulation:

Layout Extraction: Extract parasitic capacitances, resistances, and other layout-related information from the completed layout.

Post-Layout Simulation: Use extracted information to simulate the layout and verify its performance. Ensure that the circuit still operates as expected with the extracted parasites.

Layout Verification: Run DRC again after layout extraction to ensure the layout is free from manufacturing violations.

Layout vs. Schematic: Run LVS again to compare the extracted layout with the original schematic and ensure their correspondence.

Tape out: Once the layout passes all verification steps, prepare the design files for fabrication (tape out). This involves generating the necessary files, documentation, and reports for submission to the foundry.

Remember, the specific steps and considerations might vary based on target technology, design complexity, and the tools. It's essential to follow best practices, adhere to design rules, and iterate through simulations and verifications to achieve a functional and manufacturable layout for Zipper Logic-based Hybrid 1-Bit FA Circuit

4. Implementation and Results

This research section details the implementation using the suggested technique, and the implementation tools provided below:

4.1. Tool Used

The Cadence tool is used to obtain the results of this research. The Cadence tool is a comprehensive suite of EDA software used in the design and development of integrated circuits (ICs) and electronic systems. It includes a wide variety of tools that enhance many phases of integrated circuit design, such as conception, schematics capture, design of layouts, simulations, and validations. Matrix processes, charting of functions and information, procedure development, user interface design, and linking with other programming languages are all probable with Cadence. The findings provided to support the suggested effort stated below are as follows.

4.2. Performance Analysis

4.2.1. Result 1

The initial circuit simulation employs a conventional supply voltage of 0.8 V at a frequency of 1 GHz for the 16 nm production node. Afterwards, the circuits are simulated again, this time ranging from 0.4 V to 1.0 V, to study the impact of varying supply voltage on the system. Validating the input and output of the suggested finite automata is shown in Figure 2, which shows the timing pattern. The FA acts as a one-bit adder without a reduction in threshold voltage.

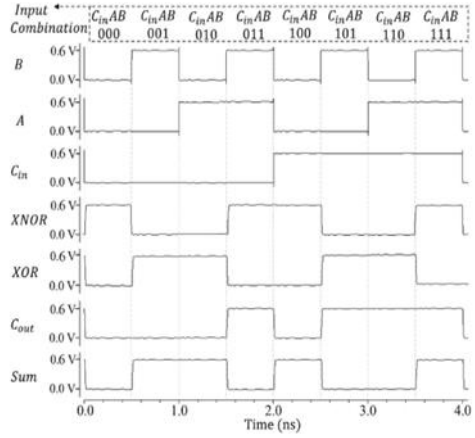

Fig 2 Input-output timing diagram for a FA

4.2.2. Result 2

First, simulations are performed at 0.8 V for both the suggested XOR-XNOR and XORXNOR modules. Table 3 displays the outcomes achieved with a supply voltage of 0.8 V. Furthermore, Figure 3-5 presents the results of a study examining the effect of changing the supply voltage on the current and proposing XOR-XNOR circuit modules. The XOR-XNOR module has higher speed and PDP performance, as shown by the data presented in Table 3 and the performance graphs depicted in Figures 3-5.

Table 3 Evaluation of 0.8 V XOR-XNOR Module Performance

XOR-XNOR module	TC	XOR	XNOR	Power (µW)
Parameshwara M.C. et al., (2017) [21]	6	9.48	8.92	0.69
Proposed	10	7.2	7.5	0.76

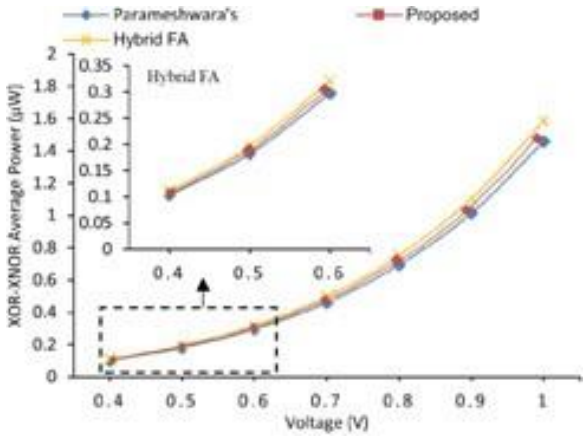

Fig 3 Power consumption analysis of XOR-XNOR modules

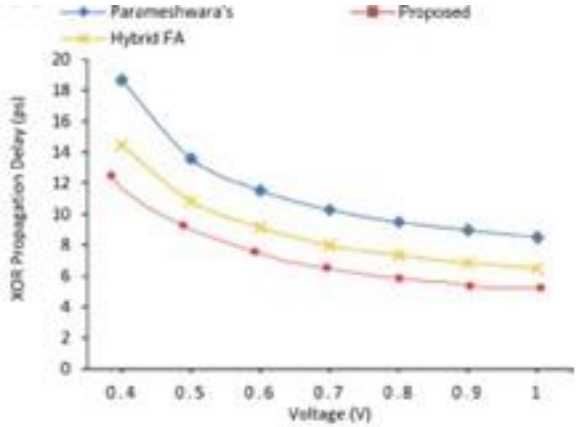

Fig 4 XOR and XNOR modules of the XOR signal's Propagation Delay are compared

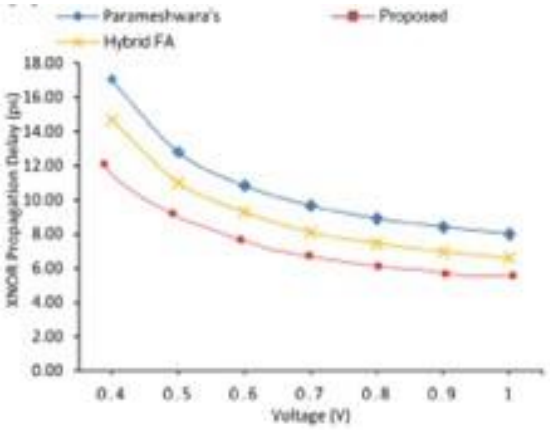

Fig 5 XOR and XNOR modules of the XNOR signal's Propagation Delay are compared

4.2.3. Result 3

Tables 4 and Figs 6 and 7 show the acquired simulation results, showing that the suggested FA circuit attained the best possible performance in AP and PDP. At advanced technological nodes like 16 nm, circuit latency is significantly affected by excessive capacitance and resistance in interconnectors and transistors. This is because high TC circuits have high input impedance and connection parasitic, both of which cause the circuit to operate more slowly.

Table 4 The functionality of FA cells with a supply voltage of 0.8 V

FA	TC	AP	PDP	Area
Parameshwara M.C. et al., (2017) [21]	16	1.47	20.68	2.61
Proposed	18	1.11	15.10	2.70

Parameshwara M.C. et al., (2017) [27] and the suggested FA exhibit low power consumption over the supply voltage range, as shown in Fig 6. This is because these layouts have a small TC. The threshold voltage drop problem, which causes additional leakage and short circuit power, is also avoided in these systems. Inverter circuits' high switching activity factor often results in more dynamic power dissipation than PT circuits. While both Parameshwara M.C. et al., (2017) [27] and the suggested design use two inverters, the latter only uses one. It could be deduced from the preceding discussion that the suggested design's leading power performance is gained because of its low TC, the absence of the threshold voltage drops problem of signals, and the reduced number of inverters. Figure 6 demonstrates that decreasing the supply voltage reduces power usage but slows down the system. The delay time increases as the supply voltage decreases due to a reduction in the available current for charging and discharging the load capacitance. The noise immunity is reduced as it is directly proportional to the supply voltage. Biomedical and many low-power Internet of Things applications are good examples of where the lower supply voltage is desirable since throughput could be compromised to save power.

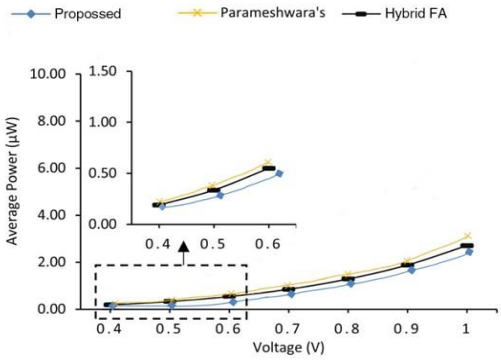

Fig 6 Comparison of Average Power FA

4.2.4. Result 4

Fig 7 displays the simple relationship between PDP and AP. The suggested FA is the most effective in terms of AP; hence, the PDP that corresponds to it would be the most effective of all the FAs considered. All four process corners have additionally verified the effectiveness of the planned FA.

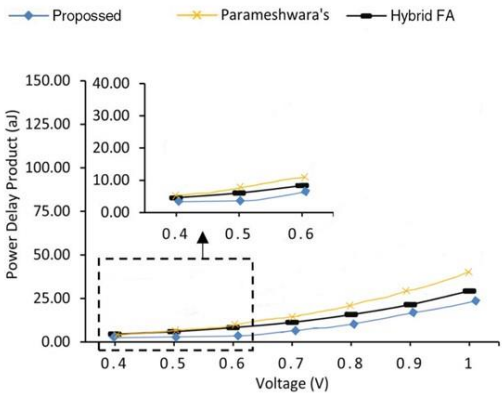

Fig 7 Power Delay Product comparison of FA

4.2.5. Result 5

An extra inverter is not required in the zipper logic with the NP block depicted in Fig. 1 since the N and P blocks are arranged in an alternative configuration. The performance of the simulation circuit may be predicted by simulating the circuit and analyzing the results in Fig. 2 as typical waveforms. The pre-charge along evaluation processes remains distinct and error-free due to the zipper logic's alternating N and P evaluation stages. As shown in Figure 8, the entire adder circuit was developed using a schematic editor in Cadence Virtuoso technology, operating at 45nm.

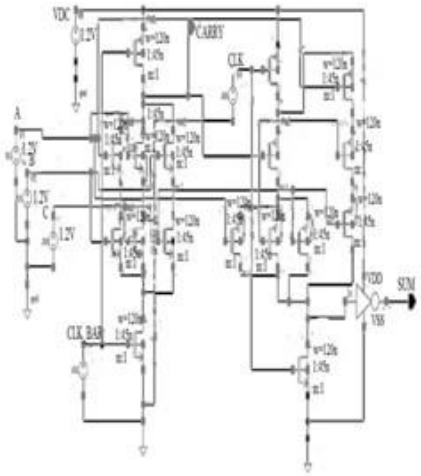

Fig 8 Final Layout of FA using zipper logic

5. Conclusion and Future Scope

The Zipper Logic-based hybrid 1-bit FA circuit design shown in this study is a significant advance in digital electronics. By seamlessly combining the characteristics of Zipper Logic approaches with traditional CMOS logic, a new circuit design paradigm develops, defined by higher speed, power efficiency, and durability. Combining Zipper Logic's fast signal propagation and dynamic logic operations with the durability of CMOS gates has proved to be powerful. The Cadence simulation results across diverse operating conditions and technology nodes demonstrate a substantial reduction in propagation delay and energy consumption compared to traditional 1-bit FA designs. This achievement is a direct result of the innovative approach that leverages the unique properties of both logical paradigms. There is also a significant performance boost compared to the best FAs currently available. As a result, the suggested FA is promising for use at the nanoscale, where it can provide great performance over the voltage range and in various other contexts.

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Author contributions

Guduru Devi Charan: Conceptualization, Methodology, Software, Field study, Visualization, Investigation. **Thumbur Gowri:** Data curation, Writing-Original draft preparation, Software, Validation., Field study, Writing-Reviewing and Editing.

Conflicts of interest

The authors declare no conflicts of interest.

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