International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Selective Harmonics Elimination Technique using Particle Swarm Optimization algorithms in Multilevel H_5 Inverter Topology

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Submitted: 04/02/2024 **Revised**: 11/03/2024 **Accepted**: 19/03/2024

Abstract: In a multilevel inverter, switching angles at fundamental frequency are obtained by solving selective harmonic elimination equations with Fourier analysis to obtain the desired fundamental voltage and eliminating certain lower order harmonics and high order harmonics with high pass filters. Since these equations are nonlinear transcendental, iterative numerical methods can solve them. In selective harmonic elimination methods, the Genetic Algorithm (GA) and Particle Swarm Optimization (PSO) algorithms have been advised for solving nonlinear algebraic trigonometric equations. Most of these techniques manipulate parameters that must be modified while maximizing fitness functions. These three fitness functions for regulating total harmonic distortion (THD) in multilevel inverters are studied. The study designed and implemented a new topology for a single-phase five-level cascaded H-bridge multilevel inverter H_5 using five switches and two DC power sources. This work aims to improve levels with few switches and sources at the output without complicating the power circuit. Lower total harmonic distortion, electromagnetic interference, and high output voltage are the new topology's key benefits. This study calculates the firing angle of switches in a single-phase five-level cascaded H-bridge multilevel inverter H_5 architecture using PSO optimization techniques to reduce lower order harmonics by raising level and employing fewer switches. The single-phase five-level cascaded H-bridge multilevel inverter H_5 architecture uses IRF 840 mosfets and STM32F407VG microcontroller. The research analyzes lower-order harmonics and THD profiles for each fitness function's modulation index. Analysis of total harmonic distortion patterns determines the best firing angle for simulation and experimentation.

Keywords—*Cascaded multilevel inverter, selective harmonics elimination techniques*

I. INTRODUCTION

Basically Inverter is a device that converts DC power to AC power at desired output voltage and frequency. Demerits of inverter are less efficiency, high cost, and high switching losses. To overcome these demerits, we are going to multilevel inverter. The term Multilevel began with the three-level converter. The concept of multilevel converters has been introduced since 1975. The cascade multilevel inverter was first proposed in 1975 [1]. In recent years multi level inverters are used high power and high voltage applications .Multilevel inverter output voltage produce a staircase output waveform, this waveform look like a sinusoidal waveform. The multilevel inverter output voltage having less number of harmonics compare to the conventional bipolar inverter output voltage. If the multilevel inverter output increase to N level [2], the harmonics reduced to the output voltage value to zero. There are two PWM methods mainly used in multilevel inverter control strategy. One is fundamental switching frequency and another one is high switching frequency. For high switching frequency classified as space vector PWM, Selective Harmonics Elimination PWM and SPWM [3].The problem of eliminating harmonics in switching converters has been the focus of research for many years. Present day available PWM schemes can be broadly classified as carrier modulated sine PWM and pre calculated programmed pulse width modulation (PPWM) schemes. If the switching losses in an inverter are not a concern (i.e., switching on the order of a few kHz is acceptable), then the sine-triangle PWM method and its variants are very effective for controlling the inverter. This is because the generated harmonics [4] are beyond the bandwidth of the system being actuated and therefore these harmonics do not dissipate power. On the other hand, for systems where high switching efficiency is of utmost importance, it is desirable to keep the switching frequency much lower. In this case, another approach is to choose the switching times (angles) such that a desired fundamental output is generated and specifically chosen harmonics of the fundamental are suppressed [5]. This is referred to as selective harmonic elimination or programmed harmonic elimination as the switching angles are chosen (programmed) to eliminate specific harmonics. This is also called as Computed Pulse Width Modulation (CPWM) or Programmed Pulse Width Modulation (PPWM)[6]. The Programmed PWM techniques optimize a

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particular objective function such as to obtain minimum losses, reduced torque pulsations, selective elimination of harmonics and therefore the most effective means of obtaining high performance results. It is interesting to note that the various objective functions are chosen to generate a particular programmed PWM technique essentially constitutes the minimization of unwanted effects due to the harmonics present in the inverter output spectra. Among these modulation methods, selective harmonics elimination (SHE) has drawn significant interest from researchers. This method is particularly appealing since it may be applied with the fundamental switching frequency, resulting in less switching losses and reduced electromagnetic interference in the drive system. The classification of harmonic profile control includes the following categories: harmonic elimination, harmonic alleviation, harmonic minimization, and total harmonic distortion. The selective harmonic removal approach [8] is utilized to achieve control over all four categories of harmonic profile[9]. To reduce the total harmonic distortion (THD) and improve the harmonic profile, one can solve the set of nonlinear transcendental trigonometric equations that reflect the output waveform of CHB-MLI [8]. By calculating these equations, the switching angles for activating the power switches can be determined. Individual H-bridge switches are activated at a specific angle and for a specific period of time[10]–[11]. The solution of such an equation using a fundamental numerical approach, such as the Newton Raphson method, sometimes incurs significant errors due to the requirement of an accurate initial guess[12]. Another approach to solving this set of equations is through the utilization of artificial intelligence (AI) algorithm techniques, including genetic algorithm[13], Particle swarm optimization algorithm[14], Gray wolf optimizer algorithm[14], Sine cosine algorithm based staircase modulation [14], gravity search optimization technique [15], BAT algorithm [16], simulated annealing algorithm, and cuckoo search algorithm [17], imperialist competitive algorithm [18]. The optimization procedure of most artificial algorithm techniques [11]–[18] requires tweaking the regulating parameters. Insufficient tuning of the optimization process can prevent convergence to the global minimum and result in errors when determining the firing angles.

In view of this, little or no difference between each one of the programmed techniques is observed when significant number of low order harmonics is eliminated. However, each one of the programmed PWM techniques is associated with the difficult task of computing specific PWM switching instants to optimize a particular objective function. This difficulty is particularly encountered at lower output frequency range due to the necessity of large number of PWM switching instants. Also in most cases only a local minimum can be obtained after considerable computational effort. Despite these difficulties programmed PWM exhibit several distinct advantages In comparison to the conventional carrier modulated sine PWM schemes which are listed below:

1. For a given inverter switching frequency, the first un-eliminated harmonic is almost double that for a natural or regular-sampled PWM scheme, thus resulting in a far superior pole switching waveform harmonic spectrum.

2. A much higher pole switching waveform fundamental amplitude is attainable before the minimum pulse-width limit of the inverter is reached.

3. About 50% reduction in the inverter switching frequency is achieved when compared with the conventional carrier modulated sine PWM scheme.

4. Higher voltage gain due to over modulation is possible. This contributes to higher utilization of the power conversion process.

5. Due to the high quality of the output voltage and current, the ripple in the DC link current is also small. Thus a reduction in the size of the DC link filter components is achieved.

6. The reduction in switching frequency contributes to the reduction in switching losses of the inverter and permits the use of GTO switches for high power converters.

7. Elimination of lower order harmonics causes no harmonic interference such as, resonance with external line filtering networks typically employed in inverter power supplies.

8. The use of pre-calculated optimized programmed PWM switching patterns avoids on line computations and provides straightforward implementation of a high performance technique.

Section II provides a description of cascaded multilevel inverter topologies. Section III covers an overview of several switching topologies used in single-phase five-level cascaded H-bridge multilevel inverters. This information describes the technique and functioning of a five-level multilevel cascaded H-bridge multilevel inverter in Section IV. Section V provides an explanation of how to decrease harmonics. The virtual instrument provides both simulation and experimental findings.

II. CASCADED MULTILEVEL INVERTERS TOPOLOGIES

A cascaded multilevel inverter made up of from series connected single full bridge inverter, each with their own isolated dc bus. This multilevel inverter can generate almost sinusoidal waveform voltage from several separate dc sources, which may be obtained from solar cells, fuel cells, batteries, ultra capacitors, etc. This type of converter does not need any transformer or clamping diodes or flying capacitors [16].Each level can generate five different voltage outputs $+2V_{dc}$, $+V_{dc}$, 0 , $-V_{dc}$ and $-2V_{dc}$by connecting the dc sources to the ac output side by different

combinations of the four switches. The output voltage of an M-level inverter is the sum of all the individual inverter outputs. Each of the H-Bridge's active devices switches only at the fundamental frequency, and each H-bridge unit generates a quasi- square waveform by phase-shifting its positive and negative phase legs switching timings. Further, each switching device always conducts for 180˚ (or half cycle) regardless of the pulse width of the quasi-square wave so that this switching method results in equalizing the current stress in each active device [17].This topology of inverter is suitable for high voltage and high power inversion because of its ability of synthesize waveforms with better harmonic spectrum and low switching frequency. Considering the simplicity of the circuit and advantages, Cascaded H-bridge topology is chosen for the presented work. A multilevel inverter has four main advantages over the conventional bipolar inverter. First, the voltage stress on each switch is decreased due to series connection of the switches. Therefore, the rated voltage and consequently the total power of the inverter could be safely increased. Second, the rate of change of voltage ($\frac{dV}{dt}$) is decreased due to the lower voltage swing of each switching cycle. Third, harmonic distortion is reduced due to more output levels. Fourth, lower acoustic noise and electromagnetic interference (EMI) is obtained. [4].

In this paper, proposed topology is the single phase five level cascaded H-bridge multilevel inverter H_5 topology which reduces number of switches as well as gives five level. In this proposed concept uses the MOSFETs semiconductor switches. MOSFETs are preferred in: High frequency applications (1MHZ), Wide line or load variations, Long duty cycles, and Low-voltage applications (500V). Mainly selected the MOSFET switches are used because of its fast switching capability [15].

Advantage of multilevel cascade inverter is following as:

(1) Bulky transformers required by conventional multi pulse inverters,

(2) Clamping diodes required by multilevel diode-clamped inverters, and

(3) Flying capacitors required by multilevel flying-capacitor inverters.

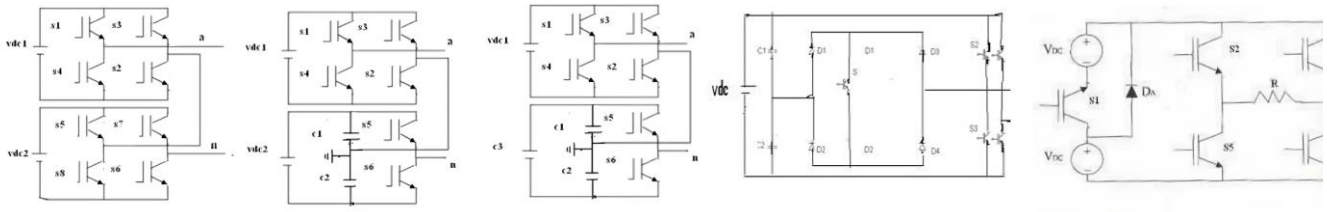
Features of multilevel cascade inverter are following as :

(1) It is much more suitable to high-voltage, high-power applications than the conventional inverters.

(2). It switches each device only once per line cycle and generates a multistep staircase voltage waveform approaching a pure sinusoidal output voltage by increasing the number of levels.

(3). since the inverter structure itself consists of a cascade connection of many single-phase, full-bridge Inverter units and each bridge is fed with a separate DC source, it does not require voltage balance circuits or voltage matching of the switching devices.

III. VARIOUS SWITCHING TOPOLOGIES OF SINGLE PHASE FIVE LEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER



(a) (b) (c) (d) (e)

Fig.1 single phase five level Multilevel cascade inverter using (a)eight switches and two sources (b) six Switches and two sources (c) six switches and single source (d) five switches and single source(e) Five switches and two source.

TABLE I COMPARISON BETWEEN DIFFERENT TOPOLOGIES WITH NEW PROPOSED METHOD OF MULTILEVEL CASCADE INVERTER

TOPOLOGIES	SWITCHES	SOURCES	CAPACITORS	DIODES
FIRST TOPOLOGIES (Fig.1(a))	8	2	-	-
SECOND TOPOLOGIES (Fig.1(b))	6	2	2	-
THIRD TOPOLOGIES (Fig.1(c))	6	1	3	-
FOUR TOPOLOGIES (Fig.1(d))	5	1	2	4
NEW PROPOSED TOPOLOGIES(Fig.1(e))	5	2	--	1

IV. PROPOSED METHOD & OPERATION OF FIVE LEVEL MULTILEVEL CASCADED H-BRIDGE MULTILEVEL INVERTER

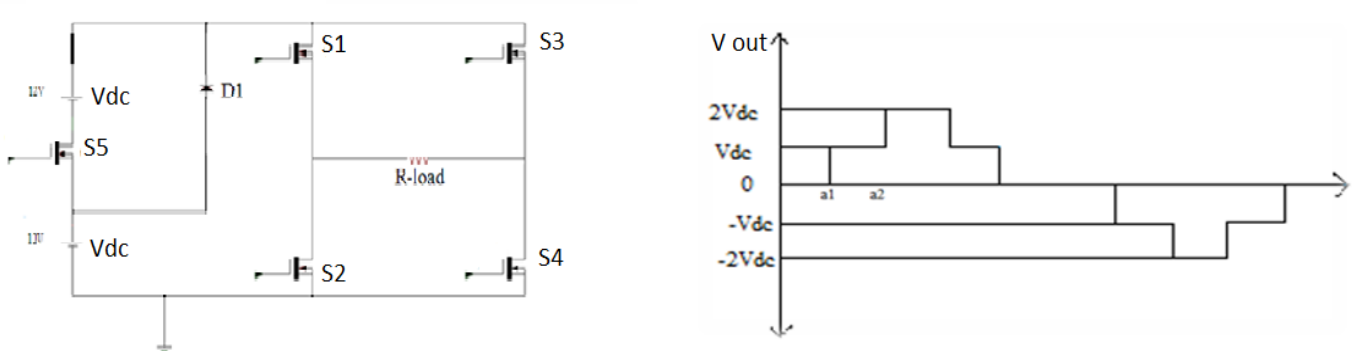


Fig. 2 proposed method of multilevel cascade inverter by using (a) five switches and two source (b) output waveform of five level multilevel inverter

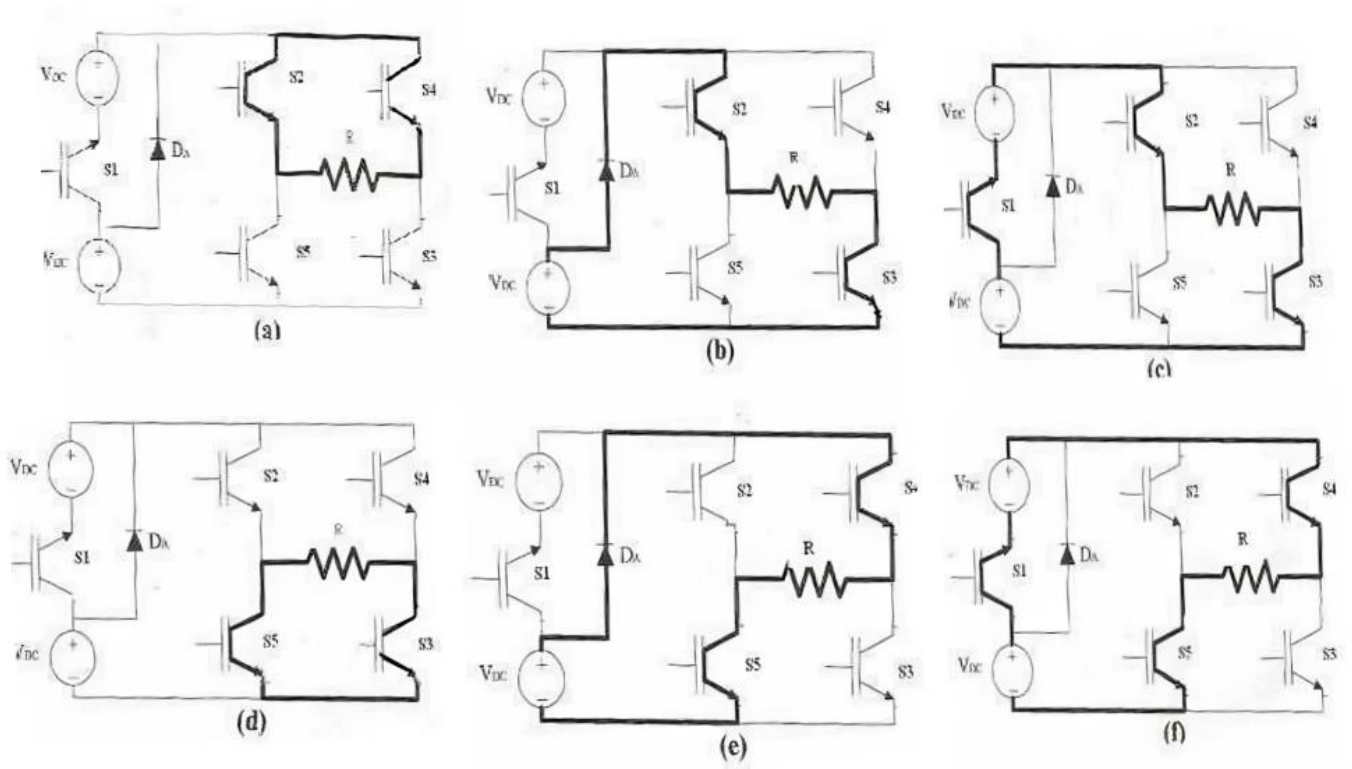


Fig.3 multilevel cascade inverter operation modes (a) 0 (b) V_{dc} (c) $+2V_{dc}$ (d) 0 (e) $-V_{dc}$ (f) $-2V_{dc}$

The circuit diagram of proposed method of multilevel cascade inverter as shown in Figure 2.The circuit diagram of operation mode with proposed method of single phase five level cascaded H-Bridge multilevel inverter is shown in figure 3 and table 2.It consists of a full-bridge inverter, capacitor voltage divider, an auxiliary circuit comprising four POWER MOSFET switches. The inverter produces output voltage in five levels: zero, $+V_{dc}$, $+2V_{dc}$, 0,- V_{dc} and $-2V_{dc}$.The advantages of the inverter topology are: Improved output voltage quality, smaller filter size, lower electromagnetic interferences, lower total harmonics distortion compared with conventional five level pulse width modulation, reduced number of switches compared to the conventional 5-level inverter. The cascaded H-bridges multilevel inverter introduces the idea of using separate dc sources to produce an ac voltage waveform. Each H-bridge inverter is connected to its own dc sourceV_{dc}. By cascading the ac outputs of each H_5 bridge inverter, ac voltage waveform is produced. By closing the appropriate switches, each H_5-bridge inverter can produce five different voltages: When a switch S_2 and S_4 of one particular H_5-bridge inverter is closed, the output voltage is 0 .When a switch S_1 and S_4 are closed, the output voltage is +Vdc. When a switch S_1 , S_4 and S_5 are closed, the output voltage is +2Vdc.. When a switch S_1 and S_3 are closed, the output voltage is 0 when a switch S_3 and S_2 of one particular H-bridge inverter are closed, the output voltage is -Vdc. When a switchS_5 ,S_3 and S_2 are closed, the output voltage is +2Vdc. The total ac voltage produced by the multilevel inverter are having five distinct voltage levels..More generally, a cascaded H_5-bridges multilevel inverter using separate dc sources can produce a maximum of S'= 4+(N-

1) distinct levels in the output phase voltage.

V. HARMONICS REDUCTION

Presence of harmonics in power system causes various problems; especially the low frequency harmonics reduce the overall efficiency of the system to a greater extent. Fourier transformation is applied in harmonic analysis. Any periodic waveform can be shown to be the super position of a fundamental and a set of harmonic components.

The output wave of a multilevel inverter can viewed as the summation of square waves having different conducting angles.

$$V_0(t) = V_a(t) + V_b(t) \quad (1)$$

Due to the quarter-wave symmetry along the x-axis, Fourier coefficients a_0 and a_n are zero.

The b_n is given as:

$$b_n = \frac{4Vdc}{\pi}\left(\int_{\alpha 1}^{\pi/2} \sin n\omega t \, d(\omega t) + \int_{\alpha 2}^{\pi/2} \sin n\omega t \, d(\omega t)\right) \quad (2)$$

$$b_n = \frac{4Vdc}{\pi} (\cos n\,\alpha_1 + \cos n\,\alpha_2) \quad (3)$$

which gives the instantaneous voltage $V_{on}(\omega t)$ of nth component as

$$V_{on}(\omega t) = \frac{4V_{dc}}{\pi}(\cos n\,\alpha_1 + \cos n\,\alpha_2)\sin \omega t \quad (4)$$

The conducting angles α_1 and α_2 can be chosen such that the total harmonic distortion of the output voltage is minimized. These angles are normally chosen so as to cancel some predominant lower frequency harmonics.

The modulation indices, denoted by M, represent the ratio of the wanted fundamental voltage to the total attainable voltage per phase.

$$M = \frac{V_1}{\frac{4V_{DC}}{\pi}} \quad (5)$$

Where, V_{DC} is DC supply, and V_1 is fundamental voltage.

Here the conducting angles should be chosen so as to eliminate the 3rd, 5th , and 7th harmonics. So we must solve the following equations.

$$\cos \alpha_1 + \cos \alpha_2 + \cos \alpha_3 = 3M \quad (6)$$

$$\cos 3\alpha_1 + \cos 3\alpha_2 + \cos 3\,\alpha_3 = 0 \quad (7)$$

$$\cos 5\alpha_1 + \cos 5\alpha_2 + \cos 5\,\alpha_3 = 0 \quad (8)$$

$$\cos 7\alpha_1 + \cos 7\alpha_2 + \cos 7\,\alpha_3 = 0 \quad (9)$$

Where, α_1, α_2, and α_3 are firing angles of for the switches. For a quarter-wave symmetrical waveform, the values of α_1, α_2, and α_3 can be anywhere from 0º to 90°.

Researchers have developed a number of fitness functions based on the aforementioned equations; these functions are then processed using AI algorithms to determine the power switch firing angles. Three Fitness functions are used to determine the firing pulses.

VI. PARTICLE SWARM OPTIMIZATION ALGORITHM (PSO)

THE CONCEPT OF PARTICLE SWARM OPTIMIZATION WAS FIRST DEVELOPED BY KENNEDY AND EBERHART IN 1995, AS DOCUMENTED IN REFERENCES [32] AND [33]. PARTICLE SWARM OPTIMIZATION INVOLVES THE FORMATION OF AN INITIAL RANDOM SWARM OF PARTICLES. A PARTICLE IS GENERATED AS IT FUNCTIONS AS A METAHEURISTIC ALGORITHM. WITHIN THE MULTITUDE OF PARTICLES, EACH INDIVIDUAL PARTICLE REPRESENTS A POTENTIAL CANDIDATE SOLUTION. WITHIN THE PARTICLE SWARM OPTIMIZATION (PSO) ALGORITHM, EVERY INDIVIDUAL PARTICLE UNDERGOES MOVEMENT TOWARDS THE ULTIMATE SOLUTION. THE VELOCITY OF THEIR MOVEMENT IS CONTINUALLY UPDATED AS THE ITERATIONS PROGRESS. EQUATIONS 18 AND 19 DETERMINE THE INTERMEDIATE VELOCITY AND POSITION OF PARTICLES, RESPECTIVELY. EQUATION 20 DENOTES THE RELATIVE IMPORTANCE OF THE PARTICLES IN EACH ITERATION. IT IS IMPORTANT TO OBSERVE THAT THE WEIGHT OF THE PARTICLE GROWS AND THE STEP SIZE DECREASES AS THE ITERATION PROGRESSES.

The intermediate velocity of the b^{th}particle in a^{th} iteration

$$V_b(a) = \omega V_b(a-1) + k_1 r_1\left[P_{best,b} - \alpha_b(a-1)\right] + k_2 r_2\left[G_{best,b} - \alpha_b(a-1)\right] \quad (10)$$

The intermediate position of b^{th}particle in a^{th} iteration

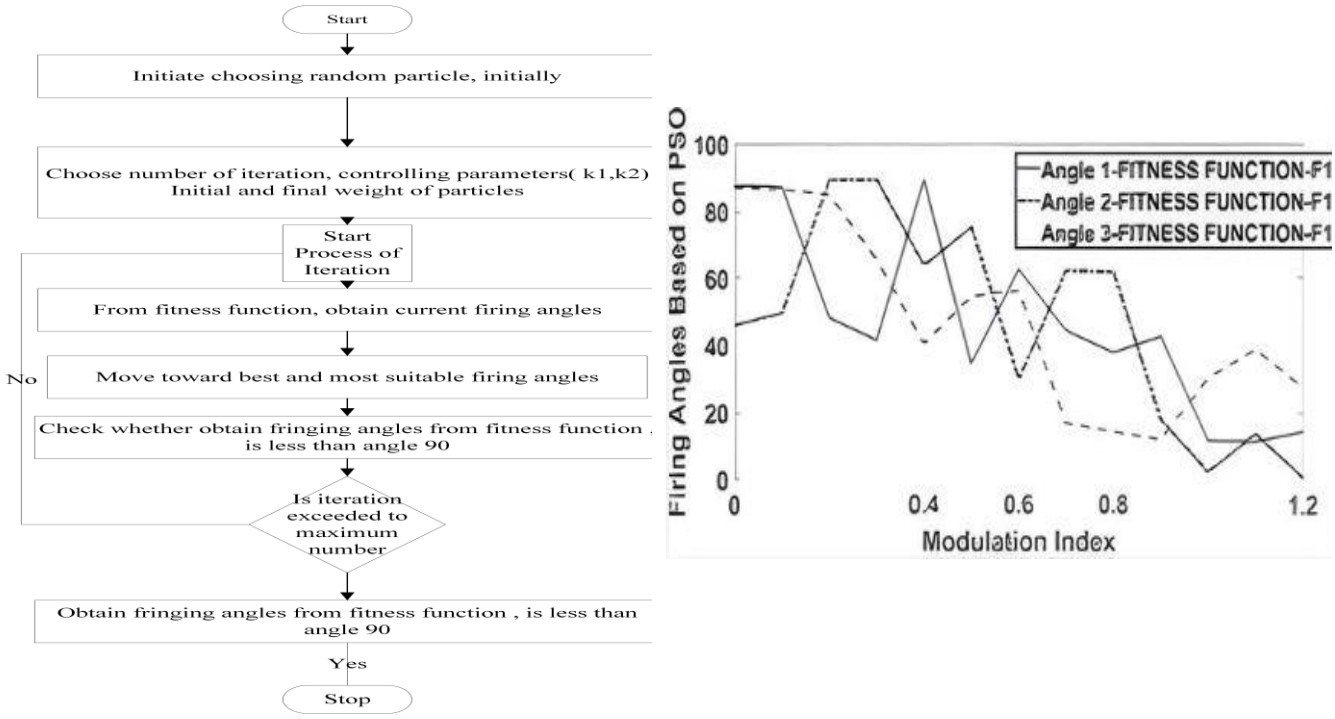
$$\alpha_b(a) = \alpha_b(a-1) + V_b(a) \quad (11)$$

$$\omega(a) = \omega_{max} - \frac{(\omega_{max} - \omega_{min})}{a_{max}} \quad (12)$$

Where, a= iteration sequence, b is 1st particle, 2nd particle,……., N particle, ω_{max} and ω_{min} are intial and final weight of particle , k_1 and k_2 are individual and group learning rates.

It is important to mention that the value of α in the fitness equations components is derived from the α value in equation 11 once the MATLAB code has completed running for the specified number of iterations. The flow chart depicted in Figure 4 outlines the sequential steps to be undertaken during the software code production process for

the PSO algorithm. It encompasses all the stages needed in preparing a code.



(a) (b)

Fig 4:(a) Algorithm flow chart for particle swarm optimization Algorithm, and(b) Firing angles based on PSO algorithm for fitnessfunction-F1

Figure 4(b) shows the relation between firing anglesobtained using the PSO algorithm versus the Modulation index. As seen from Figure 5, the utilizable firing angles are available from the modulation index value 0.4 to 1.2.

TABLE II OPERATION OF SINGLE PHASE MULTILEVEL h5 BRIDGE INVERTER

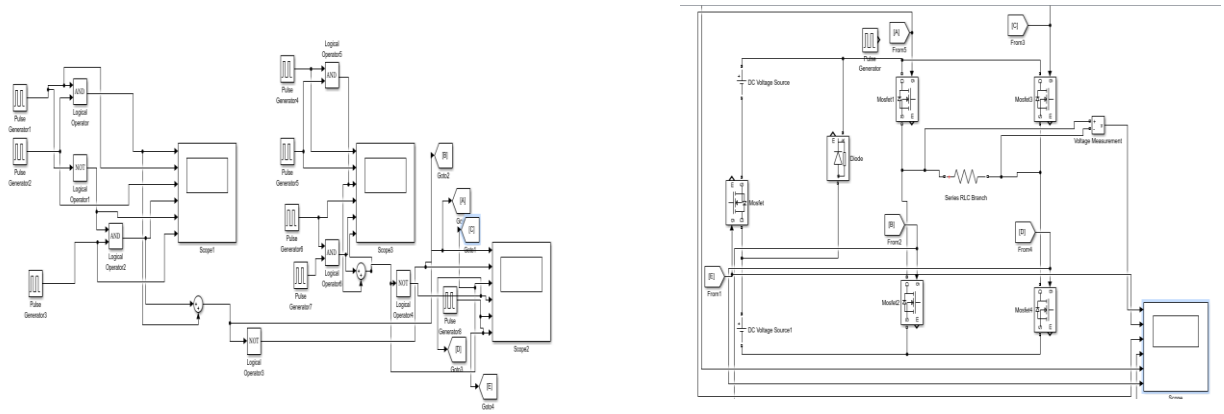
Operation	Diode	S1	S2	S3	S4	S5
0	OFF	OFF	ON	OFF	ON	OFF
+Vdc	ON	ON	OFF	OFF	ON	OFF
+2Vdc	OFF	ON	OFF	OFF	ON	ON
+Vdc	ON	OFF	OFF	OFF	OFF	OFF
0	OFF	OFF	OFF	OFF	OFF	OFF
-Vdc	ON	OFF	ON	ON	OFF	OFF
-2Vdc	OFF	OFF	ON	ON	OFF	ON
-Vdc	ON	OFF	ON	ON	OFF	OFF
0	OFF	ON	OFF	ON	OFF	OFF

Table II gives state of switch for obtaining corresponding level in multilevel inverter. For 0 Level, all switches must be turned off.

VII. Results and Discussion

The power circuit is simulated in Simulink/MATLAB by using 5 Mosfets and 100Volt 2 dc sources as shown in following fig5. The firing angle are obtained from PSO techniques:$\alpha 1 = 0.20944$ rad, $\alpha 2 = 0.837758$ rad, and $\alpha 3 = 0.947654$. The results obtained from the hardware implementation are compared to the simulation results, as depicted in figure 5 and figure 6, for the chosen scheme. The comparison is based on the Total Harmonic Distortion (THD), the output voltage obtained, and the fundamental voltage acquired by FFT analysis. Hardware testing is conducted using both lower and higher voltage levels. Lower voltage 12V batteries are used as the power source for both single phase systems..The control signals are generated from STM32F407VG.

Total Harmonic Distortion (THD) is calculated. The approach has several limitations. Firstly, it can only save a maximum of 1024 points. Secondly, the reconstructed output of the first half cycle from these points is not accurate. Lastly, the method can only acquire a maximum of two cycles from the points recorded in .csv format.



(a) (b)

Fig.5(a) Simulink gating pulse generation, and (b) Simulink power circuit of single phase H5 topology

Fig.6 Simulink results of power circuit of single phase H5 topology and gating pulse generation

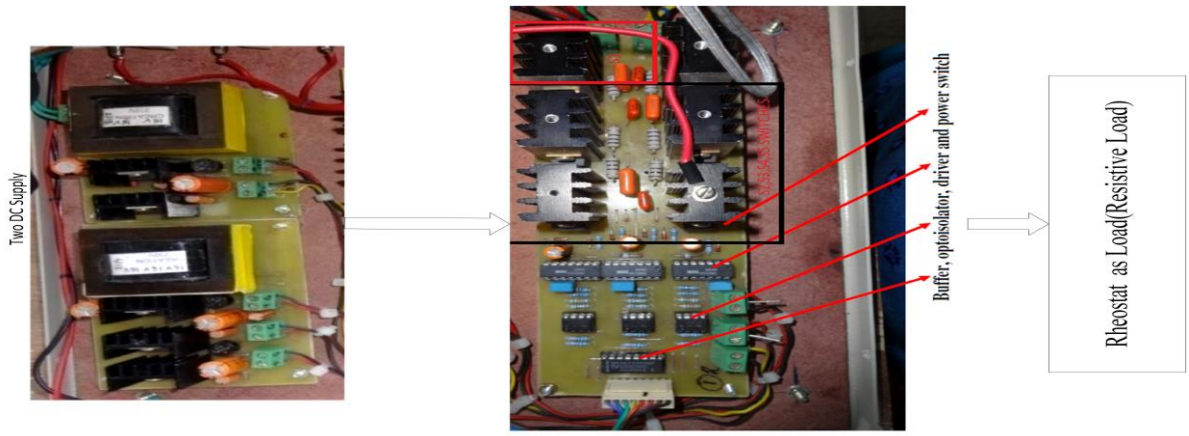


Fig.7 Experimental setup of single phase H5 topology

Figure 7 shows experimental setup of single phase H5 multilevel topology with 1Killo-ohm variable resistor to obtain five level output as shown in Figure 8

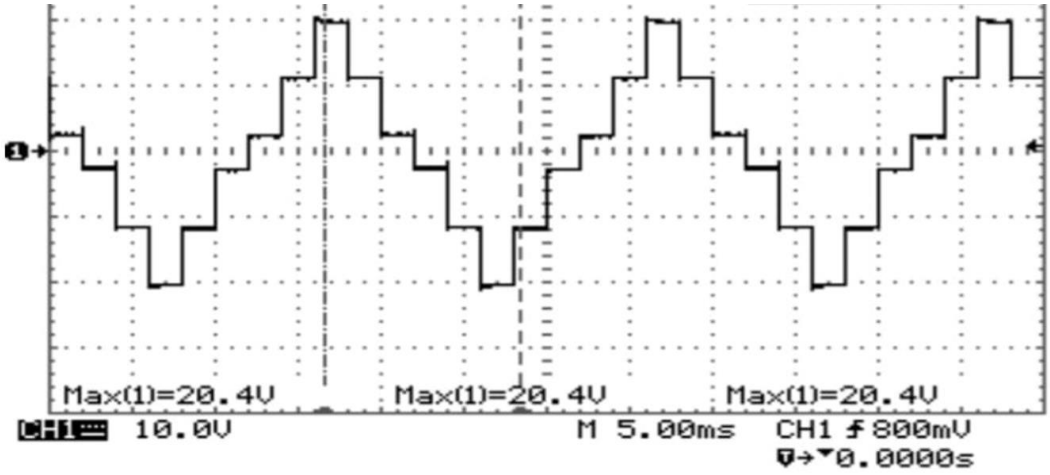


Fig.8 Experimental result of single phase H5 topology with 1Killo-ohm variable resistor

VIII. Conclusion

The experimental setup of the 5-level single-phase multilevel inverter comprises a single-phase inverter and individual H-bridge inverters and switch between two distinct dc power sources. The control signals for power electronic switches are generated using selective harmonics elimination techniques. This article compares three distinct fitness functions in terms of their performance in reducing overall harmonic distortion. Particle swarm optimization and teaching-learning based optimizer algorithms are utilized to maximize the fitness function. During the optimization process, it is noted that algorithms like PSO necessitate the adjustment of controlling parameters in order to fine-tune the parameter. There is a correlation between the results obtained from the software simulation and the experimental setup model. The harmonic analysis was conducted using the software MATLAB. The proposed work of the Single phase five level multilevel inverter has been proven to lower the total harmonics distortion of the output voltage and enhance the efficiency of the system when compared to other topologies of the single phase five level multilevel inverter.

Algorithm Performance Parameters		**Value**		
		Fitness Function -F1	***Fitness Function -F2***	***Fitness Function -F3 (Proposed novel fitness function)***
	Minimum line voltage THD value	7.54	15.88	6.22
	Modulation index for minimum line voltage THD value	1.2	0.9	1.1

PSO	Number of iterations	200	200	200
	Number of particles (Agents)	100	100	100
	Upper and lower bound	0º to 90°	0º to 90°	0º to 90°
	Number of trial for PSO code with 200 iterations	10	10	10
	Time for running the code (seconds)/trial	0.3	0.3	0.35

This work has obtained five-levels with 5 switches and 2 DC sources at the output without complicating the power circuit. It also reduced lower total harmonic distortion, electromagnetic interference, and high output voltage are the new topology's key benefits. This study calculated the firing angle of switches in a single-phase five-level cascaded H-bridge multilevel inverter H_5 architecture using PSO optimization techniques to reduce lower order harmonics by raising level and employing fewer switches.

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