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Sizing of Dual-Stage Operational Amplifiers through PVT-Aware Circuit Optimization in 0.18µm CMOS Technology

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Abstract: This study examines the effects of Process, Supply Voltage, and Temperature (PVT) fluctuations on the design of analog circuits based on CMOS technology. The paper initially discusses the impact of PVT changes on the efficiency of analog circuits based on CMOS technology. Subsequently, the text examines the enhancement of these circuits, specifically emphasizing on two-stage operational amplifier (op-amp) circuits and their efficacy in the face of PVT fluctuations. The paper explores the complex correlation between PVT variations and analog circuit design utilizing CMOS technology, emphasizing the difficulties presented by elaborate manufacturing processes, fluctuations in supply voltage, and changes in temperature. These differences have the potential to greatly modify the behavior of the circuit, which can impact the dependability and consistency of the designs. The project seeks to optimize CMOS-based two-stage op-amp circuits in order to improve their performance in different PVT settings. The cuckoo search (CS) method exhibited exceptional efficacy in circuit optimization, resulting in a notable decrease in the Total Transistor Area (TTA) to 14.12 µm². In addition, the hybrid cuckoo search particle swarm optimization (CSPSO) method demonstrated favorable outcomes, satisfying the circuit parameters requirements in 6 out of 10 separate trials. The article presents strategic optimization techniques to assist engineers and researchers in creating resilient analog systems that can efficiently adjust to dynamic PVT conditions.

Keywords: *CS, PSO, PVT, TTA*

1. Introduction

In recent years, there has been a significant increase in interest in complementary metal-oxide-semiconductor (CMOS) based analog circuit design. This is mostly due to the rising complexity and requirements associated with present integrated circuits. As the integration density increases and transistor dimensions reduce, circuit designers are becoming more concerned about the effects of three essential factors: Process (P), Supply Voltage (V), and Temperature (T) fluctuations [1-3].

Process variations arise from deviations in the fabrication process. Process parameters can vary in terms of impurity concentration amounts, oxide sizes, and diffusion depths. This results in fluctuations in the sheet resistance and characteristics of the transistor, such as the threshold voltage [4-8]. This leads to fluctuations in the width-to-length ratio (W/L) of MOS transistors. There exist five potential process corners. The five categories are referred to as typical-typical (TT), fast-fast (FF), slow-slow (SS), fast-slow (FS), and slow-fast (SF). The effectiveness of a MOS transistor is contingent upon the power supply. Fluctuations in the supply voltage impact the saturation current, which in turn influences the propagation delay of a cell. The supply voltage exhibits non-uniformity across the device, resulting in a variable propagation delay within the chip [9-15]. Temperature fluctuation is inevitable during the regular functioning of a design. During semiconductor operation, the temperature within the chip might fluctuate. This is a result of the power dissipation occurring in the MOS transistors. The primary contributors of power consumption are switching, short-circuit, and leakage power.

Multiple research have examined the influence of PVT fluctuations on analog circuits based on CMOS technology. Smith et al. [14] performed an extensive examination of the impact of process variables on circuit parameters, including gain, bandwidth, and power consumption. Their demonstration revealed that deviations from nominal circuit behavior can arise due to changes in fabrication techniques. In addition, Xu and Zhang [15] investigated the impact of supply voltage changes on the effectiveness of CMOS op-amp circuits [16]. Their research uncovered that fluctuations in the supply voltage might cause non-linearities and distortions in the circuit's response, resulting in a decline in performance in terms of linearity and dynamic range. Gao emphasized the impact of temperature fluctuations on analog circuits based on CMOS technology [17]. They noted that variations in temperature can impact the properties of transistors, resulting in alterations in circuit

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elements such as biasing currents, threshold voltages, and transconductance.

Various optimization solutions have been suggested to alleviate the impact of PVT changes on the performance of analog circuits. Gao et al. [17] proposed a new design methodology that utilizes statistical evaluation and Monte Carlo simulations to enhance the resilience of CMOS op-amp circuits against fluctuations PVT. Their method consisted of adjusting circuit settings to enhance performance metrics in different PVT conditions. In a similar vein, Zhang and Wang introduced a framework for optimizing circuit design with a genetic algorithm that takes into account PVT considerations [18]. Through a methodical examination of the range of possible designs and careful assessment of circuit performance under various process, voltage, and temperature conditions, their technique enabled the creation of durable analog circuits that are more resistant to changes. In addition, Liu et al. [19] introduced a machine learning-based optimization method for designing analog circuits that are sensitive to process, voltage, and temperature variations. By utilizing predictive modeling approaches, their approach facilitated the efficient examination of the design possibilities and selection of circuit configurations that could successfully adjust to PVT fluctuations.

Two-stage operational amplifier circuits are a crucial component in analog signal processing mechanisms, and it is extremely important to optimize their performance under fluctuations in PVT. Current studies have concentrated on creating specific optimization methods designed to address the distinct difficulties presented by two-stage operational amplifier circuits. Chen et al. [20] introduced a hybrid optimization approach that combines gradient-based approaches with evolutionary algorithms. This methodology aims to improve two-stage operational amplifier circuits for fluctuations in PVT [20]. Their approach exhibited higher performance in terms of both resilience and efficiency when compared to conventional optimization methods. In addition, Wang and Li [21] proposed a hierarchical optimization framework for the PVT-aware construction of two-stage op-amp circuits. By incorporating circuit-level and system-level optimization cycles, their approach facilitated a comprehensive analysis of design trade-offs and guaranteed dependable performance across different PVT scenarios [21-23].

To summarize, the literature review highlights the significant advancements made in optimizing circuit performance by considering PVT variations. This research specifically focuses on improving two-stage op-amp circuits in the field of analog circuits. This survey provides significant insights for engineers and researchers in the VLSI community by explaining the complex impacts of PVT variations on circuit performance [26-28]. It also showcases advanced optimization approaches. This resource offers a thorough comprehension of the difficulties presented by PVT variations and offers efficient methods to reduce their influence, hence improving the resilience and dependability of analog systems. The automated design methodology's main goal is to improve the design process in terms of cost, resilience, and performance [29-30]. PVT analysis looks for worst-case behavior scenarios across user-defined borders to make sure the circuit design satisfies all requirements and design goals, which will increase the circuit's yield and dependability [31-32]. The salp swarm algorithm (SSA) was utilized to optimize the dimensions of a CMOS differential amplifier and comparator circuit, representing a notable addition to hybrid meta-heuristic evaluation techniques in circuit design [33-34]. In order to address the changing challenges of creating adaptive analog systems in dynamic PVT settings, it is crucial to continue conducting extensive research in this subject. These improvements will unquestionably contribute to the progress of analog circuit construction and the wider field of the technology behind integrated circuits.

This research paper provides a comprehensive examination of analog circuit design using CMOS technology, with a specific emphasis on the complex factors of PVT fluctuations. The work highlights the significant influence of PVT variations on the functioning of CMOS-based analog circuits, emphasizing the immediate requirement to consider manufacturing complexities, supply voltage variations, and temperature changes in circuit design. The presence of these differences poses significant obstacles to the dependability and uniformity of analog circuits, which has led to the creation of inventive optimization solutions.

Furthermore, the study undertakes a thorough examination of the optimization of CMOS-based two-phase op-amp circuits in the presence of changing PVT circumstances. The research attempts to enhance the resilience as well as the stability associated with these circuits by introducing innovative optimization approaches. The study utilizes sophisticated simulation and analysis methods to bring useful insights to the VLSI community. It presents practical strategies to effectively manage the intricate connection between PVT changes and op-amp circuit efficiency.

2. Methodology for PVT Corner-based Circuit Optimization

PVT fluctuations are accounted for by independently adjusting the values of pressure (P), volume (V), and temperature (T) within their acceptable ranges. The resulting combinations are then analyzed and referred to as PVT corners. Contemporary designs may encompass numerous PVT corners, ranging in the hundreds or even thousands. The primary objective of PVT analysis is to determine the most unfavorable performance numbers across user-defined PVT corners. To enhance the durability

and productivity of the circuit, it is crucial to ensure that it meets all design objectives and limitations in all scenarios.

The difficulty arises in the time-intensive process of recreating each PVT corner, with the duration ranging from a few seconds to several minutes depending on the complexity of the circuit. As a result, the process of modeling all possible scenarios could take many hours or even days, creating a major obstacle in the design process. In order to overcome this problem, we employ a practical strategy by concentrating on three typical process variations, specifically TT, FF, and SS. In addition, we investigate three distinct amounts for the supply voltage and temperature, resulting in a total of 27 alternative combinations of PVT corners for examination.

Through careful selection of these specific scenarios, our objective is to demonstrate the feasibility of PVT-aware circuit design by achieving a balance between computing efficiency and thorough exploration of the design possibilities. Although this approach may not cover every conceivable PVT scenario, it provides a useful foundation for assessing circuit performance under a wide range of different operating conditions. Furthermore, it allows designers to extract vital information about the circuit's performance under various PVT variations, which aids in making well-informed decisions throughout the optimization process.

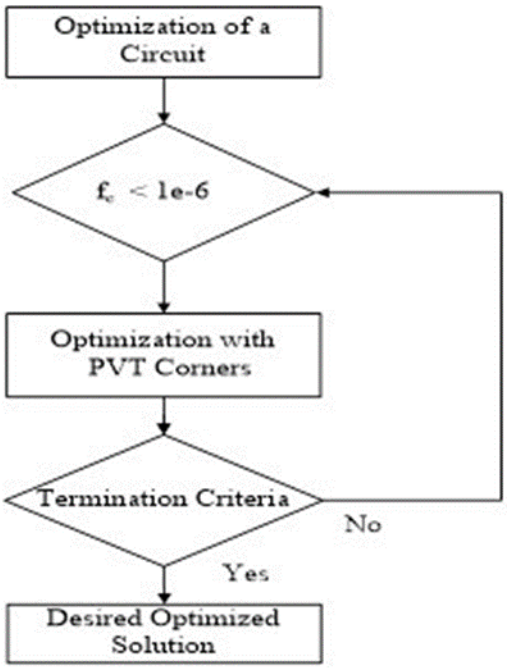

Fig. 1. Two-Step Approach for Circuit Design with PVT Variations

In essence, this focused investigation of PVT corners acts as a foundation for more resilient and durable circuit designs, paving the way for future progress in optimization techniques that take into account PVT variations. By carefully choosing and examining typical extreme scenarios, we want to simplify the process of designing analog circuits for real-life situations, while also guaranteeing their dependability and efficiency. The worst-case performance with PVT analysis is determined using a two-step approach, as seen in Figure 1.

PVT corners play a crucial role in the cyclic circuit optimization process, enabling the design of circuits while taking into account variations in process, voltage, and temperature. After optimizing the circuit using an Evolutionary Algorithm (EA) to reach the desired fitness function value, the circuit is next tested across user-defined PVT corners. The optimization process terminates when the circuit demonstrates the necessary fitness value at each established PVT corner. If the circuit fails to meet the supplied fitness conditions for any customized PVT corner, the optimizer will start a redesign iteration until the termination criteria are satisfied. The termination criteria usually consist of either achieving the maximum permissible number of loops or meeting a minimal threshold for the fitness function value. The optimization procedure persists until one of the termination circumstances is met.

This iterative optimization method guarantees that the design of the circuit is resilient and able to meet performance requirements under different PVT conditions. The optimization approach aims to obtain optimal reliability as well as performance under real-world operating situations by continuously improving the circuit design via PVT corner assessments.

As part of the optimization process, a thorough PVT analysis is performed on two-stage op-amp circuits using 0.18 µm CMOS technology. This analysis is an important stage in assessing the performance and durability of the circuits under different PVT conditions. In order to improve the optimization process, various methods such as the PSO, Hybrid CSPSO, and DE algorithms are utilized.

The work seeks to investigate various optimization techniques to examine different ways for optimizing the effectiveness of two-stage op-amp circuits considering PVT changes. The utilization of 0.18 µm CMOS manufacturing technology guarantees its applicability to current semiconductor production processes, while the incorporation of several optimization algorithms offers a thorough evaluation of optimization methods.

The work aims to use comprehensive PVT analysis and optimization with different techniques to determine the best design configurations that provide higher performance and robustness under diverse operating situations. By employing a multi-faceted approach, it becomes possible to extensively investigate the design space, resulting in the creation of sturdy and dependable two-stage op-amp circuits specifically designed for practical use in CMOS technology.

3. Optimization of two-stage op-amp with PVT corners

PVT variations are considered by independently adjusting the values of pressure (P), volume (V), and temperature (T) within their acceptable ranges. The resulting combinations are then analyzed and referred to as PVT corners. Contemporary designs may encompass a multitude of PVT corners, ranging from hundreds to thousands. The primary objective of PVT analysis is to determine the most unfavorable effectiveness values across user-defined PVT corners. To enhance the durability and productivity of the circuit, it is ensured that it meets all design objectives and limitations in various scenarios. The issue lies in the fact that the simulation of each corner can require a significant amount of time, ranging from several seconds to several minutes, depending on the circuit's complexity. Simulating all potential corners has the potential to require several hours, or even days. In this study, we have examined three process corners, namely TT, FF, and SS, along with three different supply voltage levels and three temperature values, as part of our PVT-aware circuit design proof of concept. Therefore, the number of choices for the PVT corners would be 27, which is calculated by multiplying 3 by itself three times.

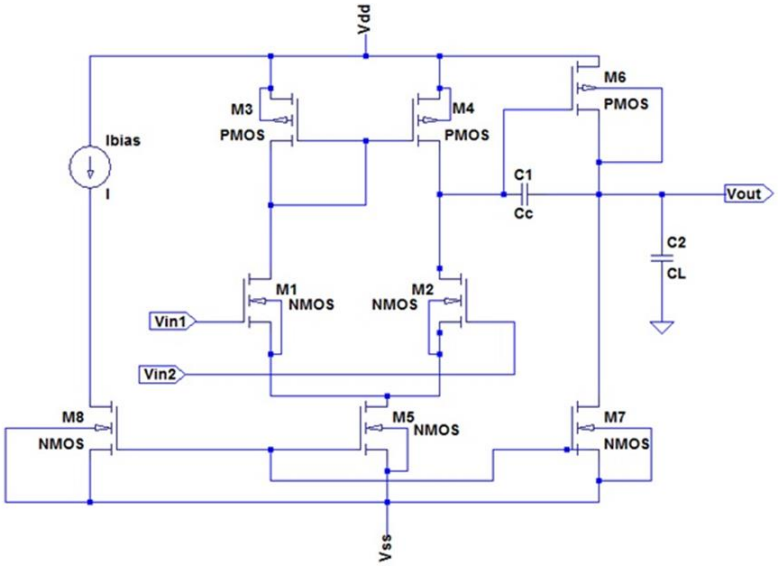

Fig. 2. Schematic of Two-stage op-amp

Furthermore, we performed optimization on a two-stage operational amplifier circuit using 0.18 µm CMOS technology under different PVT conditions. The presented investigation aimed to enhance the performance of the circuit under various PVT circumstances by utilizing advanced algorithms like as PSO, Hybrid CSPSO, and DE.

The schematic of a two-stage CMOS operational amplifier is depicted in Figure 2 [27-28]. The schematic representation of the two-stage operational amplifier stays unchanged from the previously described configuration. The optimization method involved setting specified dimensions for the transistors. The lengths of transistors M1, M2, M5, M7, and M8 were established as L1 = L2 = L5 = L7 = L8 = 0.75 µm, while the dimensions of transistors M3, M4, and M6 were set at L3 = L4 = L6 = 0.50 µm. The selection of these values was made to correspond with the properties of 0.18 µm CMOS technology and guarantee conformity with current semiconductor production procedures.

Table 1 Design parameters, search space, and optimized parameters by different EAs for Op-amp using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Design Parameters	Search Space of Design Parameters	PSO	DE	CS	CSPSO
1	$W_1 = W_2$ (µm)	1 µm to 10 µm	9.50	10.00	1.70	1.52
2	$W_3 = W_4$ (µm)	1 µm to 10 µm	7.12	6.81	3.32	3.90
3	$W_5 = W_8$ (µm)	1 µm to 10 µm	9.02	10.00	3.55	5.38
4	W_6 (µm)	1 µm to 10 µm	9.78	9.67	8.53	10.00
5	W_7 (µm)	1 µm to 10 µm	10.00	10.00	5.85	7.15
6	I_{bias} (µA)	1 µA to 10 µA	9.04	10.00	9.95	9.13

Table 2 Desired specifications and obtained specifications by different EAs for Op-amp using 0.18 µm CMOS technology at different PVT corners

Sr. No.	Specifications	Desired value	PSO	DE	CS	CSPSO
1	A_V (dB)	> 60	66.42	66.54	68.38	68.84
2	UGB (MHz)	> 10	25.55	21.51	11.81	10.83
3	PM (°)	> 45	27.90	106.20	45.19	48.71
4	+ve PSSR (dB)	> 70	81.66	80.94	80.65	81.46
5	- ve PSSR (dB)	> 70	90.06	91.62	90.75	109.84
6	RSR (V/µs)	> 10	15.69	15.07	15.42	15.11
7	FSR (V/µs)	> 10	10.89	9.95	13.70	12.25
8	CMRR (dB)	> 60	73.94	73.11	72.97	71.69
9	P_{diss} (mw)	< 1	0.07	0.07	0.11	0.10
10	N_{in} (nV^2/Hz)	< 1e-6	8.54e-08	1.37 e-07	3.51e-07	4.02 e-07
11	N_{op} (nV^2/Hz)	< 1e-4	2.40e-05	3.02 e-05	4.14e-05	4.65e-05
12	TTA (μm^2)	< 300	47.29	46.43	**19.85**	24.61

4. Results and Discussion

Table 1 presents a detailed summary of the design parameters, exploration space, and optimal parameters achieved by applying various EAs to this specific circuit using 0.18 µm CMOS technology with PVT variations. This comprehensive research allows for a meticulous evaluation of the efficacy of each optimization technique in attaining higher circuit performance under different operating situations, eventually assisting in the progress of resilient analog circuit design approaches.

Table 2 presents a thorough comparison of the targeted specifications and the specifications achieved by applying different EAs to the circuit constructed using 0.18 µm CMOS technology under various PVT variations. Every EA has the objective of maximizing the performance of the circuit based on specific criteria, including characteristics like gain, bandwidth, power consumption, and other important metrics.

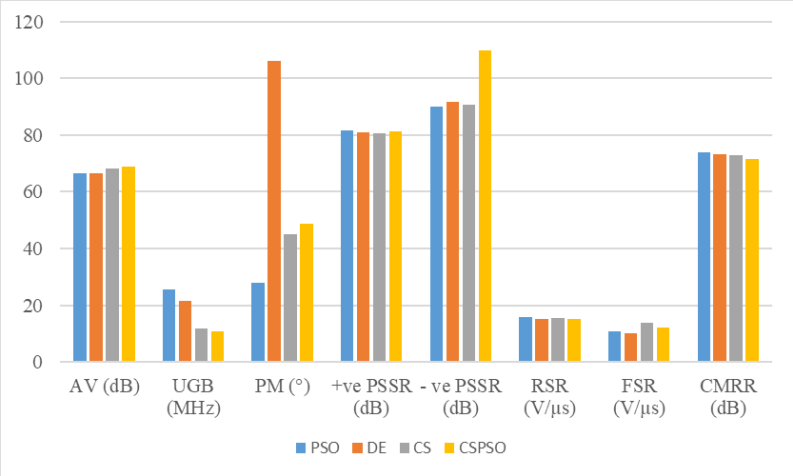

Fig. 3 Comparison of key specifications by different EAs

Table 3 Performance of different EAs for optimization of op-amp using 0.18 µm CMOS technology with PVT variations

Algorithm	$SD_{fintess}$	I_{avg}	FE_{avg}	S_{rate}	T_{sim} (s)
DE	0.378508	90.4	3030	1	4879
PSO	0.269239	100	3000	0	4765
CS	0.106352	85.30	5148	3	8140
CSPSO	0.282675	66	5970	6	9651

By comparing the acquired specifications with the desired specifications, one can gain useful insights into how effective each optimization strategy is in achieving the design objectives under various PVT settings. This investigation allows for a detailed comprehension of the advantages and constraints of each EA algorithm in attaining the best possible circuit performance in various operating situations. Figure 3 displays a comprehensive comparison of key specifications attained by implementing various EAs on the circuit built using 0.18 µm CMOS technology.

Furthermore, the incorporation of PVT variations guarantees a full evaluation of the circuit's performance, taking into consideration real-world environmental elements that could affect its operation. By conducting a thorough analysis, designers can improve their optimization methodologies and make well-informed decisions to strengthen the durability and dependability of the circuit design in real-world scenarios.

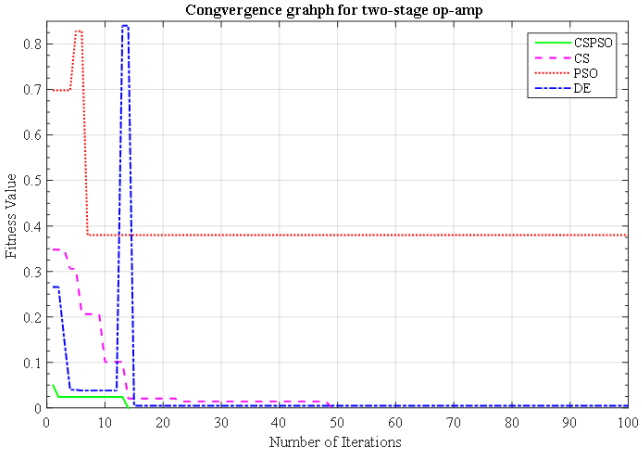

Fig. 4 Convergence graph of different EAs for two-stage op-amp optimization using 0.18 µm CMOS technology

The CS method outperformed other algorithms in optimizing this circuit, obtaining a significantly reduced Total Transistor Area (TTA) of 19.85 µm2. The effectiveness of the CS algorithm, in addition to the CSPSO, PSO, and DE algorithms, in optimizing the performance of this circuit using 0.18 µm CMOS technology is thoroughly described in Table 3.

The performance indicators of each algorithm are examined comprehensively through 10 independent runs, resulting in a robust examination of their effectiveness in reaching the required optimization targets. This comparative analysis provides a detailed overview of the strengths and drawbacks of each algorithm, helping designers choose the best appropriate optimization strategy for their individual design needs.

Moreover, by measuring the effectiveness of each method in numerous iterations, one can obtain vital information on the algorithm's stability and consistency, which can provide helpful insight for future optimization efforts. This comprehensive assessment highlights the significance of choosing the right algorithm to get the best possible performance in circuit design, ultimately leading to breakthroughs in analog circuit design approaches.

The CSPSO algorithm achieved the given criteria in 6 out of 10 independent runs, demonstrating significant performance in meeting the specifications for the circuit. Similarly, the CS algorithm found success on three occasions, whereas the DE approach only succeeded once. Unfortunately, the PSO algorithm failed to meet all parameters in any of the runs.

Furthermore, an examination of the mean iteration counts throughout the 10 separate trials indicated that each of the CSPSO and CS algorithms necessitated less repetitions in comparison to the DE and PSO algorithms. This observation indicates that the CSPSO and CS algorithms demonstrate greater effectiveness in descending towards the best possible result during the optimization process for this specific circuit.

Therefore, it may be inferred that the CSPSO and CS algorithms outperform the DE and PSO algorithms in meeting the desired parameters for this circuit. This demonstrates the efficacy of the CSPSO and CS algorithms in efficiently exploring the design space and enhancing circuit parameters, emphasizing their potential to be the best optimization methods for similar circuit design situations.

Figure 4 represents the convergence paths of the CS, CSPSO, DE, and PSO algorithms while optimizing the two-stage operational amplifier using 0.18 µm CMOS technology. Figure 4 analysis illustrates that the CSPSO algorithm displays significantly faster convergence towards the desired fitness value when compared to the DE, CS, and PSO algorithms. The rapid convergence trajectory of the CSPSO method indicates that it efficiently investigates and takes advantage of the design space, quickly determining the best circuit configurations that fulfill the specified performance requirements.

The convergence graph offers vital information into the performance and effectiveness of each algorithm for optimization in exploring the optimization space. Through visual comparison of the convergence behaviors of several algorithms, designers can gain valuable insights into their individual strengths and limitations. This enables more informed choices when selecting algorithms for future optimization work.

Moreover, the rapid convergence of CSPSO highlights its potential as a favored optimization method for comparable circuit design situations. Quick convergence of the algorithm towards the desired fitness value not only improves efficiency but also speeds up the overall design procedure, allowing for faster iterations and speedier achievement of optimized circuit designs.

5. Conclusion

The main objective of this study was to optimize circuit design by considering the effects of PVT variations. The goal is to create a design that meets specific requirements under all possible PVT conditions defined by the user. The optimization of two-stage operational amplifier circuits was carried out using 0.18 µm CMOS technology over 27 distinct PVT corners. Multiple metaheuristic EAs were utilized to get the required values.

The performance of each EA in the context of PVT-aware design for two-stage op-amp circuits was thoroughly investigated through rigorous experimentation and optimization. The results of the present work highlighted the higher performance of the CS and CSPSO algorithms compared to the DE and PSO algorithms in the field of PVT-aware circuit optimization.

Furthermore, our investigation demonstrated that the CS and CSPSO algorithms consistently beat their competitors, indicating improved efficiency and effectiveness in navigating a complex area that includes several PVT corners. This comparison assessment provides insight into the positive and negative aspects of each optimization method, assisting practitioners in choosing the best appropriate approach for PVT-aware circuit design problems.

In summary, this work provides useful insights into optimizing PVT-aware circuits, emphasizing the significance of choosing suitable optimization methodologies to guarantee reliable circuit performance under different operating situations. Designers may easily overcome the obstacles caused by PVT changes in modern CMOS technology by utilizing powerful metaheuristic algorithms like CS and CSPSO. This enables the construction of resilient and reliable analog circuit designs.

Conflicts of interest

The authors declare no conflicts of interest.

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