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Design Optimization of SiC-CMOS Inverter for Space Applications

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Abstract The ever-increasing requirements of integrated circuits in space application demands critical research for new devices/circuits, which have potential to withstand Single Event Effect (SEE) under radiation environments. Lightweight satellites require high-density integrated circuits. Currently, silicon based CMOS ICs are used for this purpose. Goal of the proposed work is the design optimization of SiC-CMOS IC and to study its performance in high temperature conditions and in the space radiation environment. In this work, feasibility studies on the performance validation such as IV characteristics, switching characteristics, gain and voltage transfer curve of SiC-MOSFET and SiC-CMOS inverters are carried out in TCAD simulations (COGENDA) for space applications. The optimized design parameters and performance parameters will help us to develop the SiC-CMOS based physical ICs for future ISRO space crafts.

Keywords: *Silicon carbide, Complementary Metal Oxide Semiconductor inverter, Single Event Effect, Voltage Transfer Curve, High Radiation Environments.*

1. Introduction

The reliable operation of on-board electronic systems in spacecraft is crucial due to the increasing number of space missions. On-board electronic circuits are frequently exposed to radiation, thermal cycling, and extreme temperatures [1], such as the range of temperatures on the lunar surface from −183 °C to 127 °C [2]. Conventional radiation shielding and thermal control setups are necessary for electronic circuits fabricated by Silicon technology to withstand the harsh space environment. Additionally, size and weight are critical factors for on-board electronic circuits. Wide bandgap materials, particularly silicon carbide (SiC), offer resilience in space environments. SiC is a compound semiconductor composed of 50% Silicon (Si) and 50% Carbon, with covalent bonds of Si-C that have significantly higher binding energy (4.6 eV) compared to Si-Si bonds (1.8 eV). Popular SiC polytypes include 3C-SiC, 4H-SiC [3,4], and 6H-SiC, as shown in Figure 1.

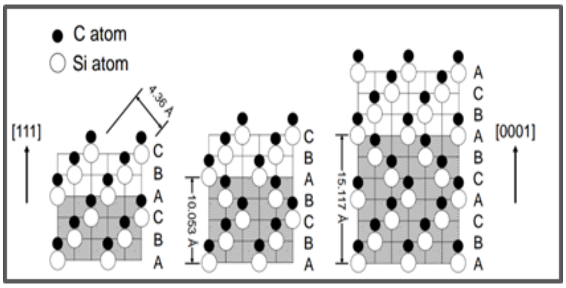

Fig 1: Crystal Structure in SiC: (a) 3H-SiC, (b) 4H-SiC, (c) 6H-SiC.

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The increasing popularity of SiC in space applications is attributed to its high breakdown voltage, high electron saturation drift velocity, higher power and current densities, low on-resistance, higher switching frequency, and high operating temperatures. SiC circuits do not require additional heat-sinking management due to their higher thermal conductivity and stability. This technology offers a lower cost and a smaller footprint solution for high-temperature applications. Table 1 presents a comparison of the electronic properties of Si and SiC.

Table 1: Properties of Silicon and Silicon Carbide semiconductor materials [5].

Property	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV at 300K)	1.12	2.4	3	3.2
Critical electric field (V/cm)	2.5x	2x	2.5x	2.2x
Thermal conductivity (W/cm.K at 300K)	1.5	3-4	3-4	3-4
Saturated electron drift velocity (cm/s)	1x	2.5x	2x	2x
Electron mobility (/Vs)	1350	1000	500	950
Hole mobility (/Vs)	480	40	80	120
Dielectric constant	11.9	9.7	10	10

SiC is positioned to replace Si in various electronic applications due to its exceptional characteristics. It offers higher break-down voltage than silicon, minimal leakage current, and rapid switching, making it a compelling choice for power electronic applications. The new generation SiC transistors with low on-resistance and high switching speed present a practical solution for designing high-frequency DC/DC converters.

2. Simulation and Comparative Analysis for MOSFET (Si and SiC):

In this work, a systematic simulation study and comparative analysis for the characteristics of N-MOSFET for Si & SiC are carried out using the TCAD (COGENDA) simulation tool [6] as shown in Figure 2.

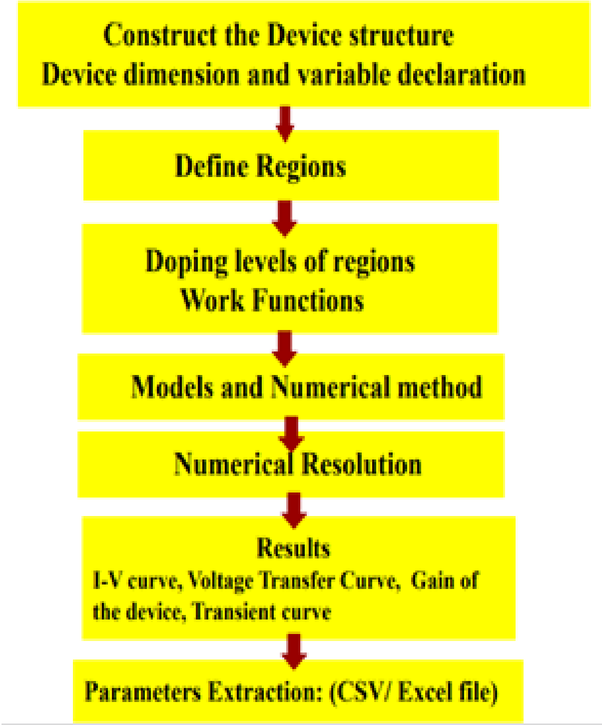


Fig 2: Flowchart of Simulation work in COGEND [6].

The N -MOSFET in SiC technology with design parameters as listed in table 2, has been constructed in COGENDA simulation framework and it is compared with conventional Si-substrate N-MOSFET as shown in Figure 3 Si (left) and SiC (right).

Table 2: design parameters of N-MOSFET of SiC in simulation.

Sr. No.	Parameter	Value
1.	Channel Length	<5 um
2.	Oxide Thickness	5nm
3.	Substrate doping concentration	6 x 10^{17} cm^{-3}
5.	N+ (Source and drain doping concentrations)	1 x 10^{20} cm^{-3}
6.	Work function of NMOS	4.1 eV

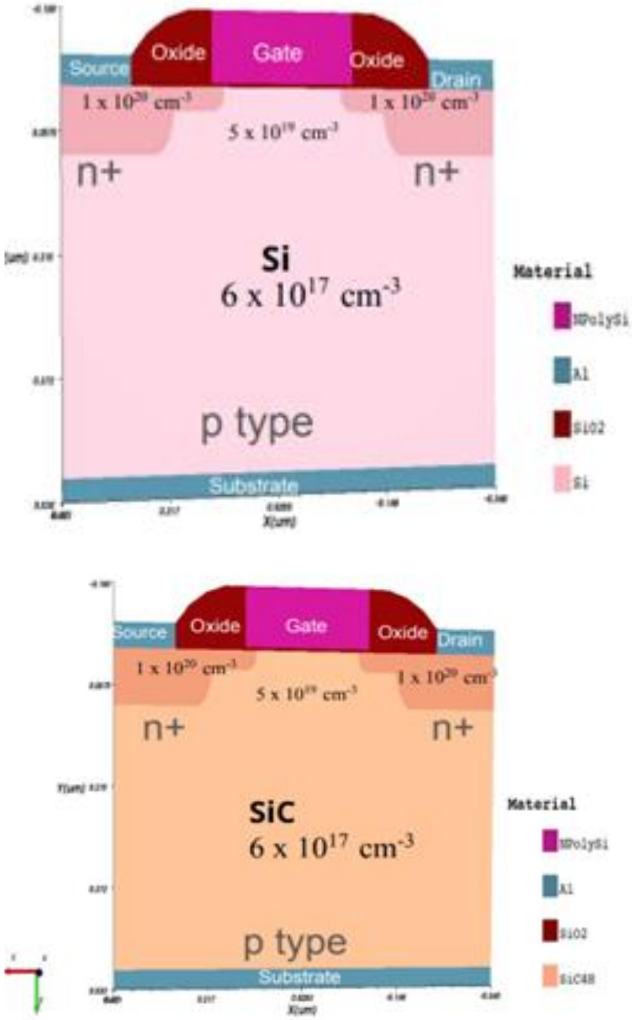


Fig 3: N MOSFET Si-Substrate (left) N MOSFET SiC-Substrate (right).

3. Results

The operation mode of MOSFET depends on gate-voltage and drain-source voltage. The voltage of the substrate can be also changed to manipulate the threshold voltage of MOSFET. The behaviour of MOSFET can be seen in I-V characteristics. The results of Drain current (I(DS) as a function of drain voltage (V(DS)) are shown in Fig. 4 for N channel MOSFET. We can clearly see that the threshold voltage of SiC MOSFET is higher than the Si MOSFET. Thus, leakage current will be less in SiC MOSFET than Si MOSFET, which is an important feasibility study for SiC MOSFET operation.

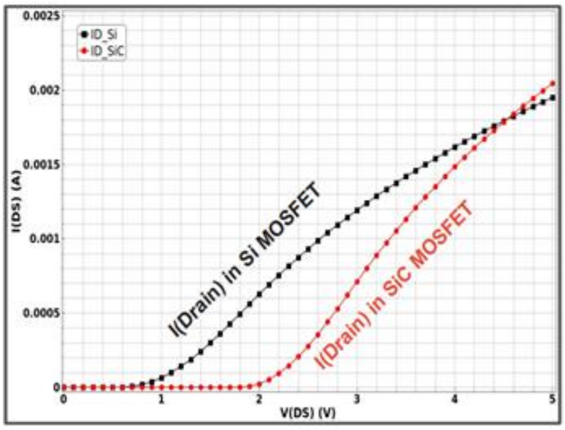


Fig 4: I (DS) vs V(DS) for N MOSFET: Si (black color), SiC (red color).

Further, to validate the performance of SiC N-MOSFET, I(DS) current vs V(DS) voltage is studied for different Gate voltage (V(GS)) and results are compared with Si N MOSFET, as shown in Fig 5.

As expected, on increasing the drain voltage in MOSFET, the drain current increases for different gate voltages for both Si (left) and SiC MOSFET (right), which confirms our feasibility study for SiC MOSFET in simulations.

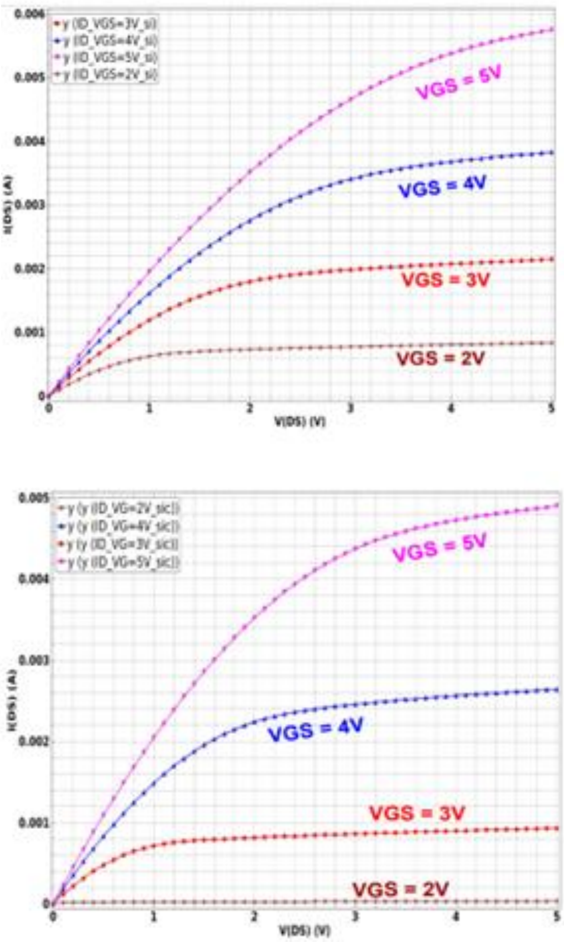


Fig 5: I(DS) vs V(DS) for different gate voltages (V(GS)) for N-MOSFET with Si-substrate (left) and SiC substrate (right).

Further, total ionizing dose effect is studied on SiC-NMOSFET and results are shown in Fig 6. On increasing the total ionizing dose, the threshold gate voltage decreases due to trapped charges, which is expected.

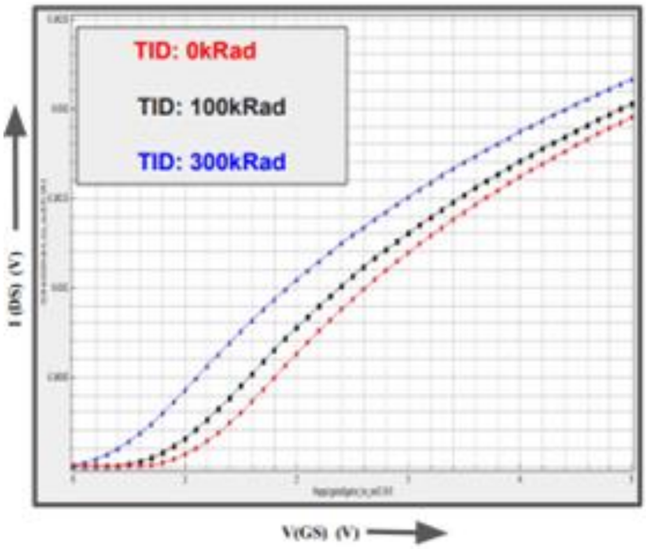


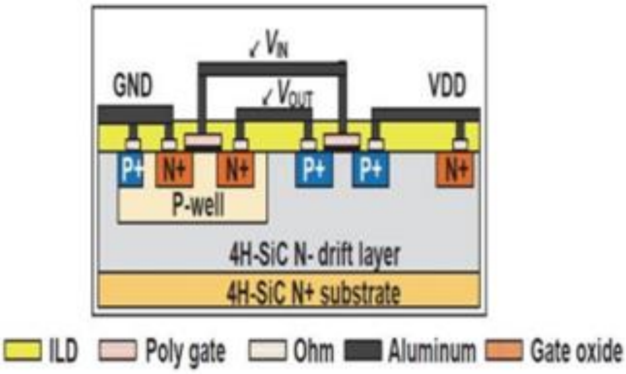
Fig 6: I(DS) vs V(GS) for different total ionizing doses (TID) for NMOSFET SiC.

4. Simulation and Comparative Analysis of CMOS Inverter (SiC and Si)

In this work, a systematic simulation study and comparative analysis for the characteristics of CMOS inverter with Si & SiC substrate are carried out using the COGENDA simulation tool. The SiC CMOS inverter using the design parameters as listed in table 3 is constructed in COGENDA simulation platform as shown in Fig 7.

Table 3: Design parameters of SiC CMOS inverter in simulation.

Sr. No.	Parameter	Value
1.	Channel Length	< 5um
2.	Oxide Thickness	5nm
3.	Substrate doping concentration	$6 \times 10^{17}\ cm^{-3}$
4.	Source and drain doping concentrations	$5 \times 10^{19}\ cm^{-3}$
5.	N+ (Source and drain doping concentrations)	$1 \times 10^{20}\ cm^{-3}$
6.	Work function of NMOS	4.1 eV
7.	Work function of PMOS	5.1eV
8.	Width of the PMOS	3 x NMOS



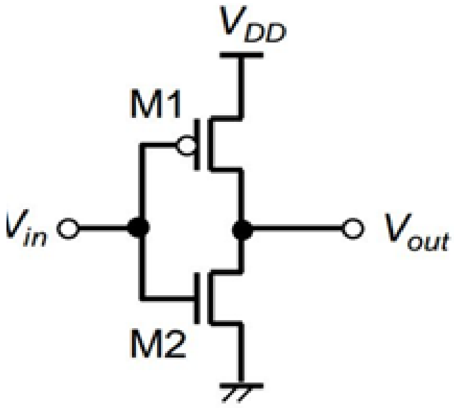
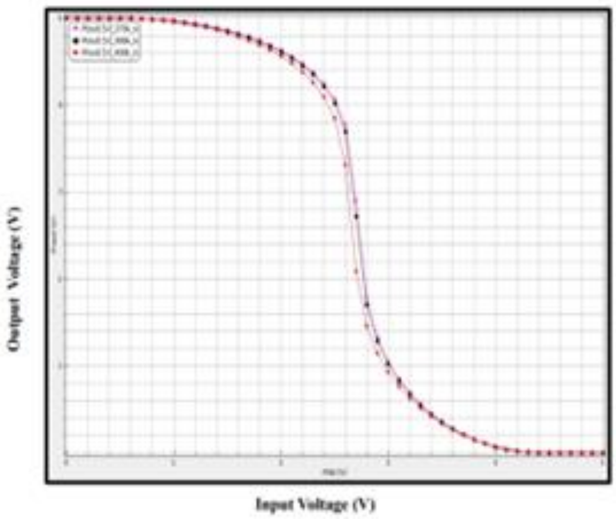


Fig: 7: SiC CMOS Structure (left) SiC CMOS circuit (right).

5. Results

The simulated voltage transfer curve (VTC) CMOS inverter is shown in Fig 8. As can be seen from Figure, the VTC curve is sharper in case of SiC CMOS inverter (right) in comparison to Si CMOS Inverter (left), which is expected. This shows that dynamic power consumption in SiC CMOS inverters is lesser as compared to Si CMOS inverters. This lower switching loss in SiC CMOS inverter makes it suitable for high frequency application during space travel.



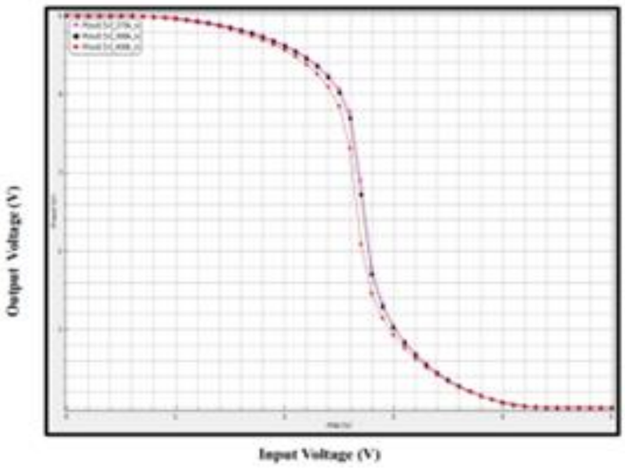


Fig 8: Voltage Transfer Curve: Si CMOS inverter (left), SiC CMOS inverter (right).

Further, Gain of CMOS inverter is studied as a function of input voltage for SiC and compared with Si CMOS inverter and corresponding results are shown in Fig 9.

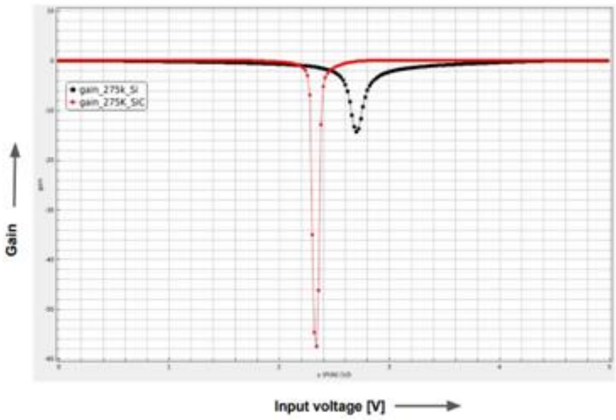


Fig. 9: Gain as a function of input voltage for CMOS Inverter: Si (black color) and SiC (red color).

For analog applications, SiC CMOS amplifiers give higher gain in comparison to Si CMOS amplifiers. The Switching characteristics (transient curve) are obtained for SiC CMOS Inverter and compared with Si CMOS Inverter and results are shown in Fig 10. We can see faster switching of SiC CMOS inverter in comparison to Si CMOS inverter, which makes it suitable for high frequency application during space travel.

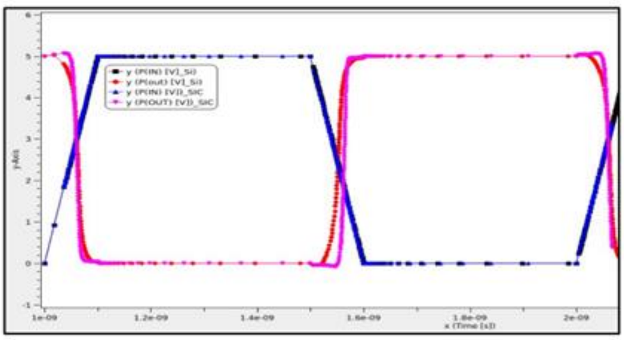


Fig 10: Transient response of SiC and Si CMOS inverter

6. Summary and Conclusions

A systematic comparative analysis for the characteristics of two important devices (Si and SiC: N-MOSFETs and CMOS inverters) have been carried out using COGENDA simulations at MNIT Jaipur. We observe the expected performance from MOSFET studies that higher voltage is required to switch 'ON' the SiC MOSFET as compared to the Si MOSFET. Further, higher drain current is observed in SiC MOSFET as compared to Si N-MOSFET. It provides good performance for power device applications. We also observe the expected results from the CMOS Inverter. The dynamic power consumption in SiC CMOS inverter is less as compared to Si CMOS inverter. This lower switching loss in SiC CMOS inverter, which makes it suitable for high frequency application during space travel. Further, it is also seen that for analog application, SiC CMOS amplifiers give higher gain in comparison to Si CMOS amplifiers.

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