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Design and Simulation of 8-Bits Arithmetic Logic Unit (ALU) For Inverter Applications

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Abstract — In this paper, an 8-bit ALU (Arithmetic Logic Unit) for 3V operation has been designed. Numerous mathematical and logical operations can be carried out using the ALU**.** The central processing unit (CPU), memory unit, and input/output unit are the fundamental components of a computer. The CPU of a computer is essentially the same as a human brain. The ALU, control unit, and all of the registers are included. All design were simulated using Tanner EDA tool v12.5 in 32nm 0.5 technology. Performance analyses were done with respect to power, delay and power delay product.

Keywords*— Inverter, Full Subtractor, Multiplexer Tanner Tool V_12.5.*

Introduction

Functionally, an ALU can be divided up into three circuits: the arithmetic circuit, the logic circuit and the shift circuit[1]. i)The arithmetic circuit performs typical arithmetic operations such as addition, subtraction and increment or decrement by one [2]. The basic component of an arithmetic circuit is the Full adder. By using a multiplexer to control the data inputs to the adder [3], it is possible to obtain different types of arithmetic operations [4-7]. Depending on the selection inputs and the input carry, the arithmetic circuit can generate [8]. the different arithmetic micro-operations listed **Table 1.**

S1	S0	Cin	Input	Output	Micro operation
0	0	0	B	A+B	Add
0	0	1	B	A+B+1	Add with cry
0	1	0	B’	A+B’	Sub with borrow
0	1	1	B’	A-B	Sub
1	0	0	0	A	Transfer A
1	0	1	0	A+1	Increment by 1
1	1	0	1	A-1	Decrement A by1
1	1	1	1	A	Transfer A

Table 1: Function table of the arithmetic Circuit

ii) The ALU, logic circuit performs the basic logic micro-operations: NOT, AND, OR and XOR. From these four micro-operations all known logic micro-operations can be derived. Figure 5-2 shows the logic diagram for one stage of logic circuit. The four gates generate the four logic operations and the multiplexer select the desired operation as shown in **Table 2.**

S1	S0	Output	Operation
0	0	AB	AND
0	1	A+B	OR
1	0	A⊕B	XOR
1	1	A’	Complement

Table 2: Function table of the 2-bit Logic Circuit.

iii) Shift circuit used to perform the shift micro-operations. The contents of a register can be shifted serially to the left or to the right. The shift circuit contains multiplexers as shown in Figure 5-3. when the select line is 0 the 4-bit input data

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are shifted right. When the select line is 1 the input data are shifted left. There are two serial inputs one for shift left and other one for shift right. The function **Table 3** shows the outputs of the multiplexers in each case**.**

S	H3			
	H3	H2	H1	H0
0	IR	A3	A2	A1
1	A2	A1	A0	IL

Table 3: Function table of the 4-bit Shift Circuit

Block Diagram for Designing of ALU

ALU design by following the correct procedure some introductory part is given as**,** Making the programming, draw the schematic diagram, and for the layout diagram at each and every step check the DRC for the proper designing. The design of the 8-bit ALU is based on the use of a carry select line, implemented using AMI's C5N process. Once verification was completed parasitic were extracted. To create a test for finding the maximum operating frequency a pseudo-random input stream was applied to each input of the ALU and observed the circuit during the input transition. If the switching of the transistors takes longer than the period of the input then the ALU may give a erroneous output. **Fig 1** shows the step-by-step procedure for the ALU designing.

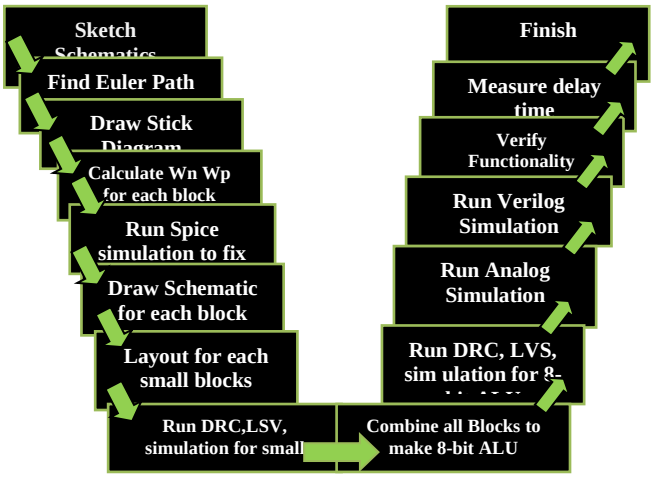

Fig1: Block Diagram of ALU Design

MODULE

There are different modules use for the designing of the ALU, schematic and waveform (DC and AC Analysis) some of them are as follows.

Simulation and Results

I) Inverter

An inverter or NOT gate is a logic gate which an inverter circuit outputs a voltage representing the opposite logic-level to its input. Inverters can be constructed using a single NMOS transistor or a single PMOS transistor coupled with a resistor. Since this 'resistive-drain' approach uses only a single type of transistor, it can be fabricated at low cost. However, because current flows through the resistor in one of the two states, the resistive-drain configuration is disadvantaged for power consumption and processing speed implements logical negative.

The truth table is shown in **table 2.**

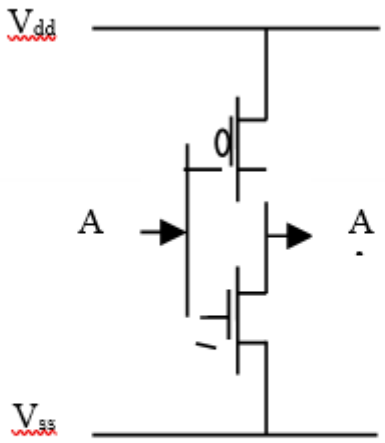

Fig.2: Structure of inverter.

INPUT	OUTPUT
A	NOT A
1	0
0	1

Table 2. Truth table of inverter.

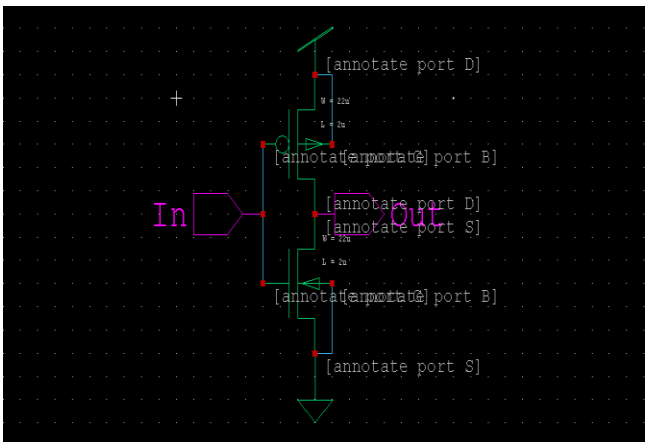

Fig.3 Schematic diagram of Inverter.

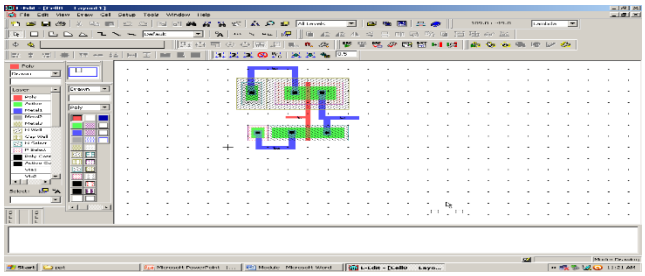

Fig. 4 Layout of Inverter.

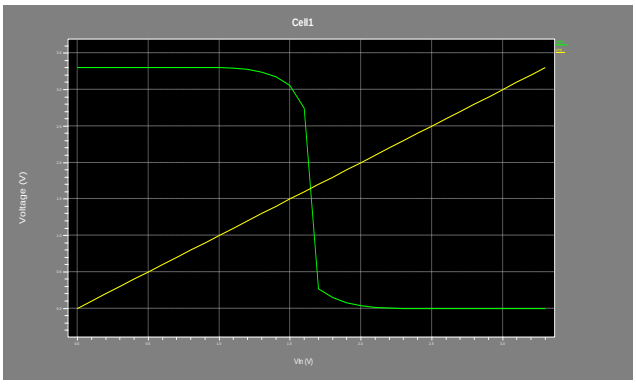

Fig. 5 DC analysis of Inverter.

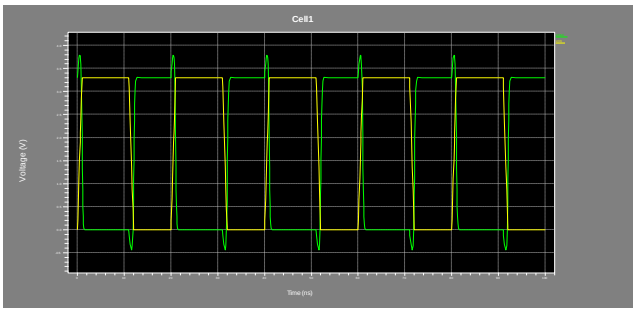

Fig. 6 AC analysis of Inverter.

II) Full_ Adder

In ALU, full adder forms the core of the entire design. The full adder performs the computing function of the ALU. A full adder could be defined as a combinational circuit that forms the arithmetic sum of three input bits. It consists of three inputs and two outputs. In our design, we have designated the three inputs as A, B and Cin. The third input Cin represents carry input to the first stage. The outputs are SUM and CARRY [9-10]. **Figure 7** shows the logic level diagram of a full adder. The Boolean expressions for the SUM and CARRY bits are as shown below.

$$SUM = A \oplus B \oplus Cin$$

$$CARRY = A \cdot B + A \cdot Cin + B \cdot Cin$$

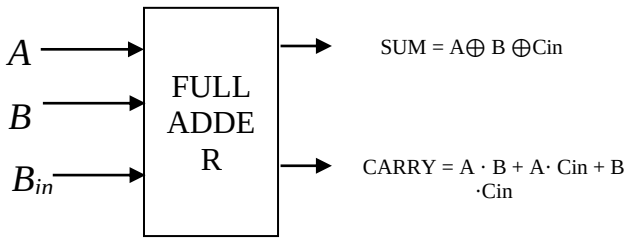

Fig. 7 Block diagram of Full_ Adder.

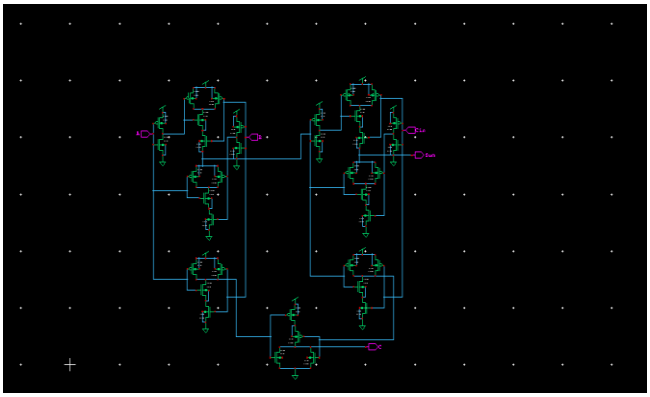

Fig. 8 Schematic diagram of Full_Adder.

III) Full Subtractor

Full Subtractor is a combinational circuit with three inputs A, B and $B_{in\ and}$ two outputs Difference(D) and Borrow (B_0) [13].

$$D = A \oplus B \oplus B_{in}$$

$$B_0 = A'B_{in} + A'B + BB_{in}$$

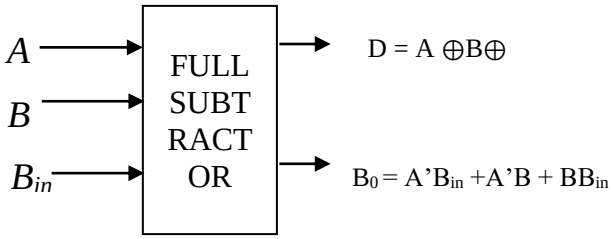

Fig. 9 Block diagram of Full_Subtractor

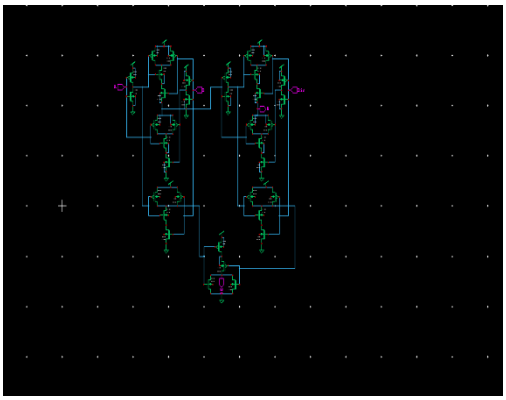

Fig. 10 Schematic diagram of Full Subtractor.

IV) Multiplexer

M**ultiplexer** (or **MUX**) is a device that selects one of several analog or digital input signals and forwards the selected input into a single line.[1] A multiplexer of 2^n inputs has n select lines, which are used to select[11].

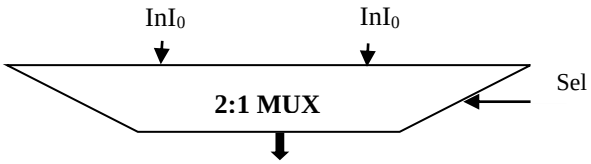

Fig. 11 Block of 2:1 MUX

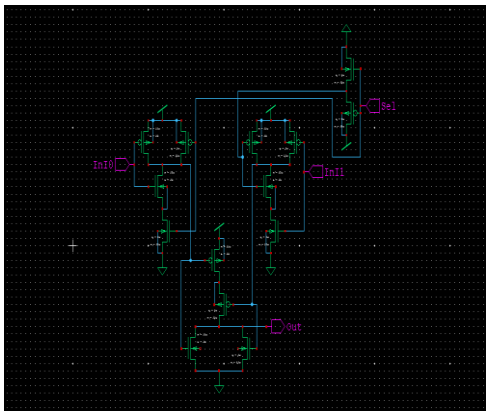

Fig.12 Schematic diagram of Multiplexer_21.

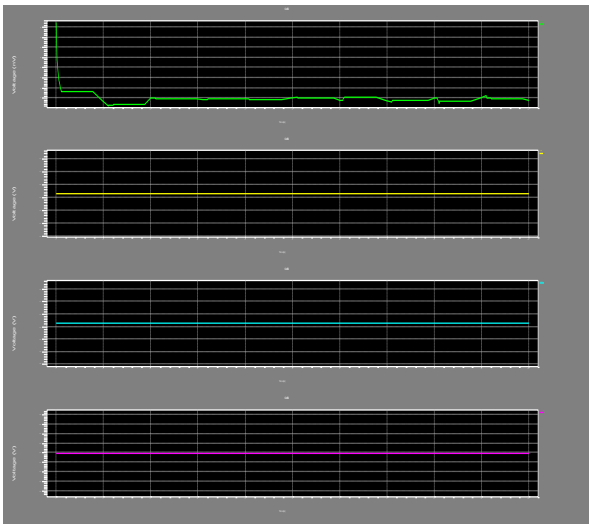

Fig. 13 DC analysis of Multiplexer_21.

V) Arithmetic Logic Unit

A 8-bit ALU has been designed for 3V operation. The ALU can perform various arithmetic and logical operations**.** The basic blocks of a computer are central processing unit (CPU), memory unit, and input/output unit. CPU of the computer is basically the same as the brain of a human being. It contains all the registers, control unit and the arithmetic logic unit (ALU). ALU considered as the most important subsystem in a digital computer. An arithmetic logic unit (ALU) is a digital circuit which performs arithmetic, logic and shift operations on two n-bit digital words. Functionally, an ALU can be divided up into three circuits: the arithmetic circuit, the logic circuit and the shift circuit. The 8-bit ALU was formed by combining four Full Adder and four Full Subtractor with five multiplexers as shown in the schematic diagram.

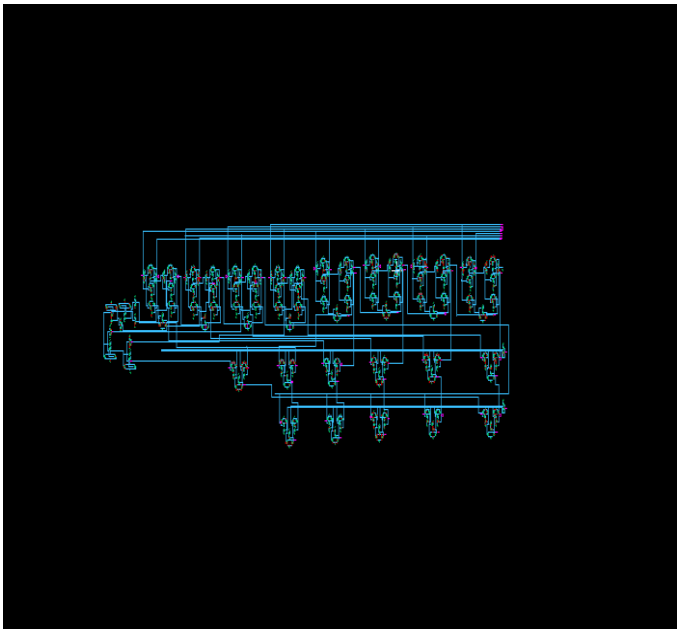

Fig. 14 Schematic diagram of ALU.

SPICE Coding

.Model NMOS NMOS kp=4.5u vto=1v gamma=0.4 lambda=0.02 phi=0.6v

.Model PMOS PMOS kp=3.6u vto=-1v gamma=0.4 lambda=0.02 phi=0.6v

Vdd Vdd Gnd 3.3v

Vin In Gnd Pulse(0 3.3v 0 1n 1n 10n 20n)

.tran 1n 100n

.dc VIn 0 3.3v .1v

.Power Vdd 1n 100n

.print V(In A) V(In B) V(In C) V(In D) V(In E) V(In F) V(In G) V(In H) V(select 0) V(select 1) V(Out A) V(Out B) V(Out C) V(Out D) V(Out E)

* SPICE export from S-Edit 12.50 Fri May 25 15:34:05 2012

Design: ALU Design1.sdb

* Cell: Cell25

* View: view0

* Export as: Top-level Cell

* Netlist port order: default

* Exclude .model : no

* Exclude .end: no

* Expand paths: yes

* Root path: C:\Users\haneef\Desktop\ALU\ALU Design1.sdb

* Exclude global pins on subcircuits: no

* Export control property name: SPICE

* Wrap lines: no (to 0 characters)

MMOSFET_P_257 N_326 N_105 Vdd Vdd PMOS L=0.5u W=1.5u AD=1.8p PD=5.5u AS=1.8p PS=5.5u

MMOSFET_N_65 Gnd N_54 N_146 N_152 NMOS L=0.5u W=0.5u AD=0.6p PD=3.5u AS=0.6p PS=3.5u

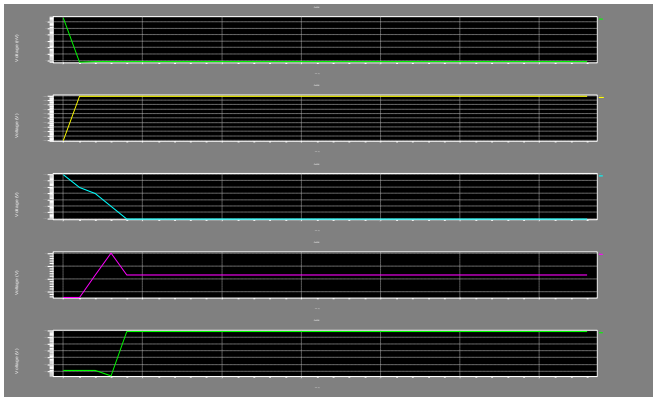

Fig. 15 DC analysis of ALU.

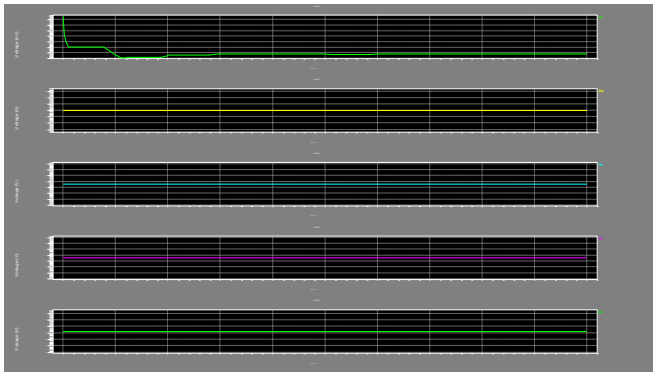

Fig. 16 AC analysis of ALU.

Conclusion

Tanner EDA Tools V12.5 with 0.5 sub-micron technology was used to develop the suggested ALU, and an analog design environment was used for simulation. The output waveforms' operational correctness was confirmed, and the voltage levels were examined. By employing the shorted-gate mode of the ALU in circuits that do not affect the delay, the suggested design can be further enhanced for better power usage. A multiply and accumulate (MAC) unit, which is widely used in signal processing, can be created by manipulating a modified multiplier and KSA. In reference [8], for designs larger than 32-bit. It can be used in place of a modified ALU after optimization. It is possible to conduct additional hardware analysis, such as layout simulation to examine the die area used for various components.

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