International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Design and Performance Analysis of 8051 Microcontroller with 0.5 Technology for Low Power Applications

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Submitted: 25/10/2022 **Revised:** 14/12/2022 **Accepted:** 04/01/2023

Abstract: - In this paper, the innovative power getting is analyzed which minimizes the power dissipation in submicron circuits. The overall view this paper is to attain high speed, low power with alternative logic cells that lead to have reduced power dissipation. Here the total components are designed sub micro technology and observed that power analysis. This paper describes the implementation of a digital controller using an 8051 microcontroller and an active power line conditioning system to enhance the power quality in the distribution network. This study investigates the 8051 microcontroller's susceptibility to basic power analysis attacks. We have designed the Schematic and Layout of 8051 microcontroller, using tanner Tools (v12.5) and 0.5 sub-micron Technology. We have also done the transient Analysis and DC analysis of above-mentioned components using Tanner Tools (v12.5).

Keywords - *8051 Microcontroller, Modelsim (SE-4a), Tanner tools (V12.5), 6 -Transistor based RAM) and Xilinx (6.1i).*

1. Introduction

As we know that the 8051 microcontroller is the most popular general-purpose microcontroller in use today. In this paper we have Analysis of 8051 microcontroller using CPU, RAM and interrupt controller before 8051 microcontroller design on VHDL Language in which check only waveform but we design on Tanner tools (v12.5) and VHDL both and analysis of DC and AC of 8051 microcontroller. We have drawn the schematic of all these three components using Tanner Tools from the schematic we study the Transient and DC analysis of the above-mentioned components. Beside that we have also drawn tools and 0.5 sub-micron technology.

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2. Central Processing Unit OF 8051 Microcontrollers

The Central Processing Unit (CPU) is the brain of the 8051 microcontroller that performs bulk of data-processing operations. In modern computational clusters these issues are usually prevented with the help of jobs and job schedulers, which postpone a job and schedule it later, when resources available [2]. **Figure 1** shown the CPU architecture that we used drawing its schematic and layout using Tanner EDA tool V12.5.

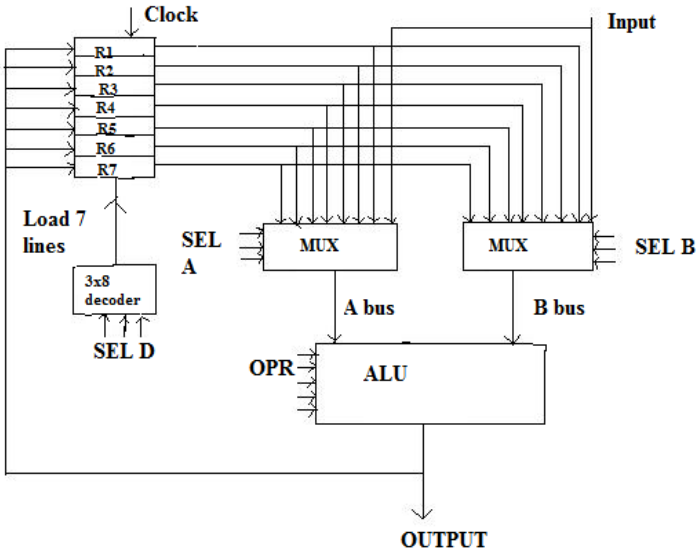

Figure1: Architecture of CPU

3. 6-Transistors Based RAM

In this paper we have considered 6 Transistor based RAM. In this RAM out of Six Transistors are used as two inverters and the remaining two transistors are controlled by Word Line Figure (2) shows the circuit diagram of 6T Based RAM. A 128-byte internal asynchronous RAM and other synchronous peripherals including interrupts [3]. Using this, we have drawn schematic of using tanner tools. In addition to local RAM for storing intermediate results and specialized state machines to manage point addition and doubling operations, they implemented field arithmetic operations in hardware. This method has a significant hardware cost even though it is very quick (no operand transfers occur during a point addition or doubling) [13-15]. Internal and external program memory access as well as external RAM memory access were tested separately. The correct operation of the timers, interrupt system, and serial port was then confirmed. Random program testing was then carried out to confirm that the core behaved correctly on test cases that would have gone unnoticed in earlier stages of verification [16].

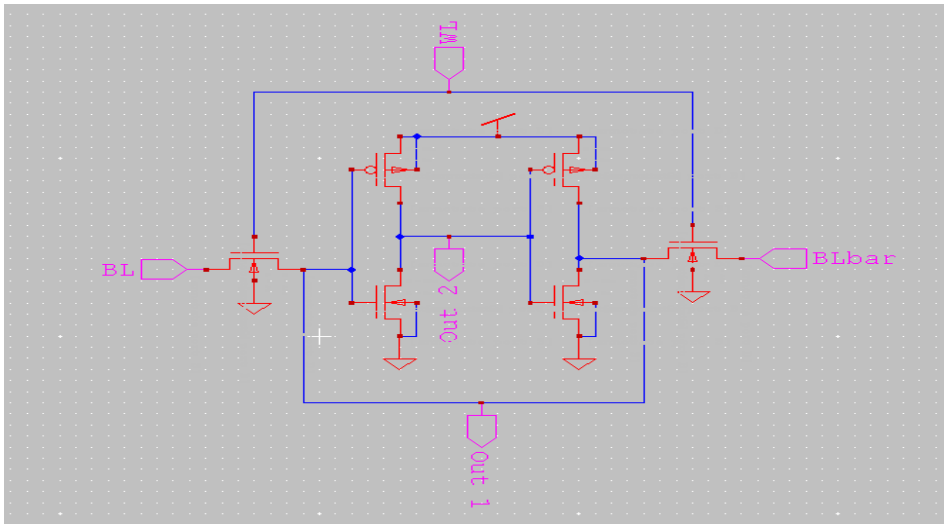

Figure 2 Circuit diagram of RAM

4. Interrupt Controller

Interrupt Controller is a component used to increase the speed of CPU. The Microcontroller includes the SPARC Processor an FPU, a memory controller, an Interrupt Controller and Peripheral devices in a single-chip [4,9-12]. **Figure 3** shown the circuit diagram of interrupt controller using D- Flip - Flop. We have used this circuit diagram to design

schematic of Interrupt Controller using Tanner EDA Tool V12.5. **Figure 3** Circuit diagram Interrupt Controller.

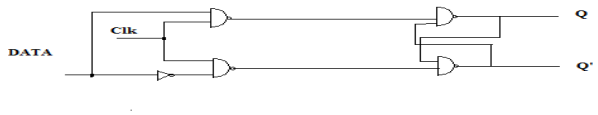

Figure 3 Circuit diagram of D-Flip Flop.

5. Simulation and Results

5.1 Layout of RAM

Using Tanner EDA Tool V12.5, we have designed the schematic and Layout of RAM**.** of RAM after doing simulation on Tanner Tool V12.5. **Figure 4**.

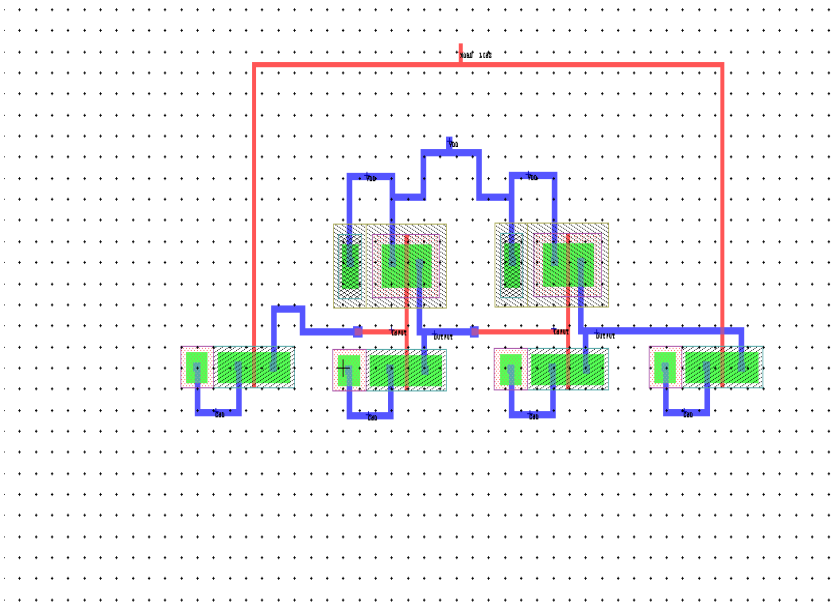

Figure.4 Layout of RAM

5.1.1 Transient & DC analysis of RAM

We have done the Transient and DC analysis of RAM using tanner tool V12.5. **Figure 5** Shown the DC analysis of RAM.

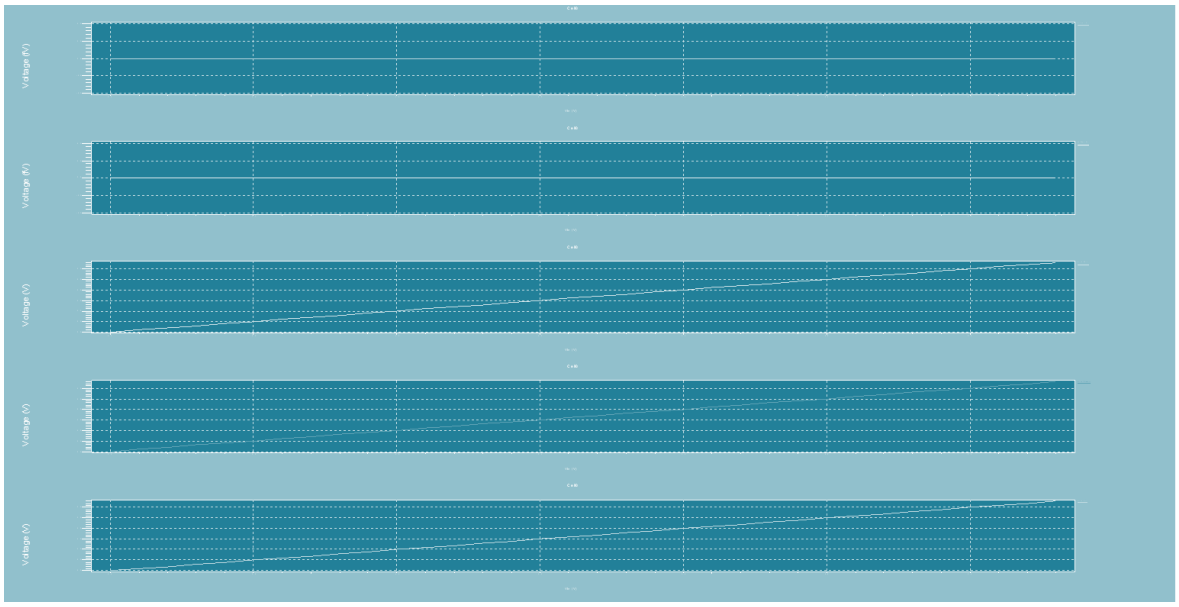

Figure 5 DC Analysis of RAM

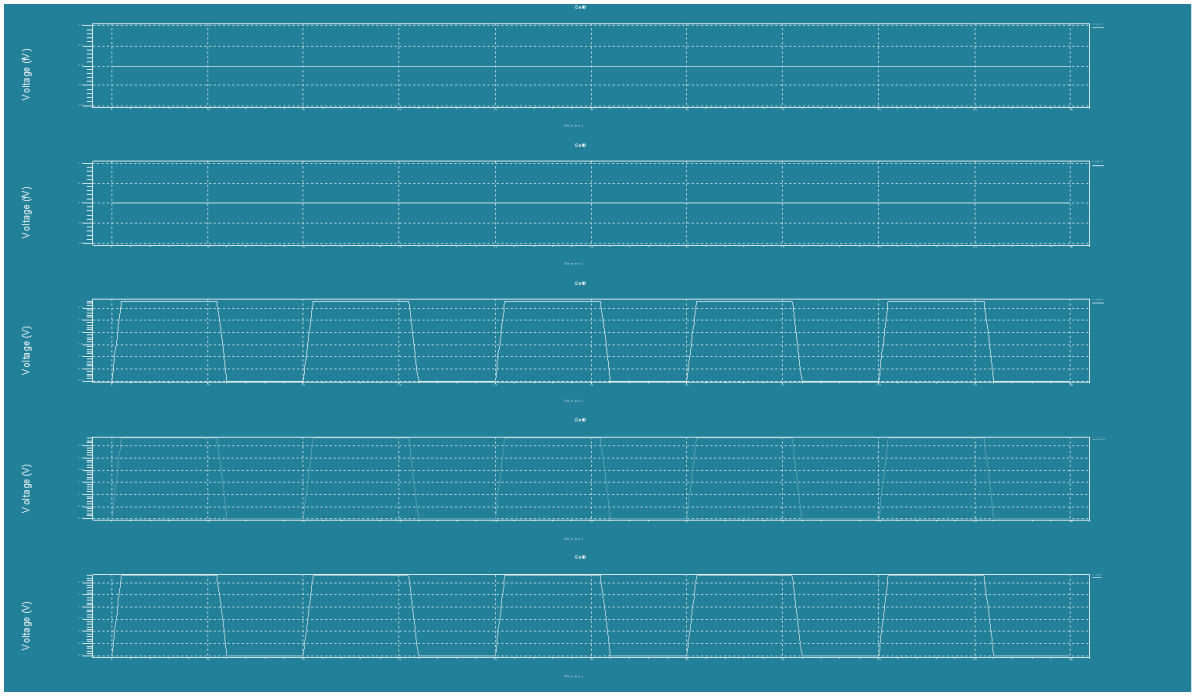

Figure 6 Transient Analysis of RAM

5.2 Schematic Diagram of Interrupt Controller

Figure 7 shows the schematic diagram of interrupt controller designed using Tanner EDA Tool V12.5.

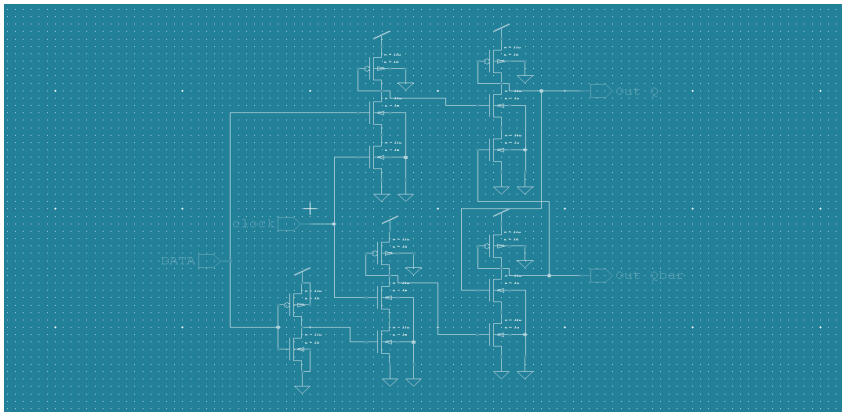

Figure7 Schematic diagram of Interrupt controller

5.2.1 Transient & DC Analysis of Interrupt Controller

Figure 8 & **Figure 9** shows the simulation results of Transient and DC analysis of Interrupt Controller using Tanner EDA Tool V12.5.

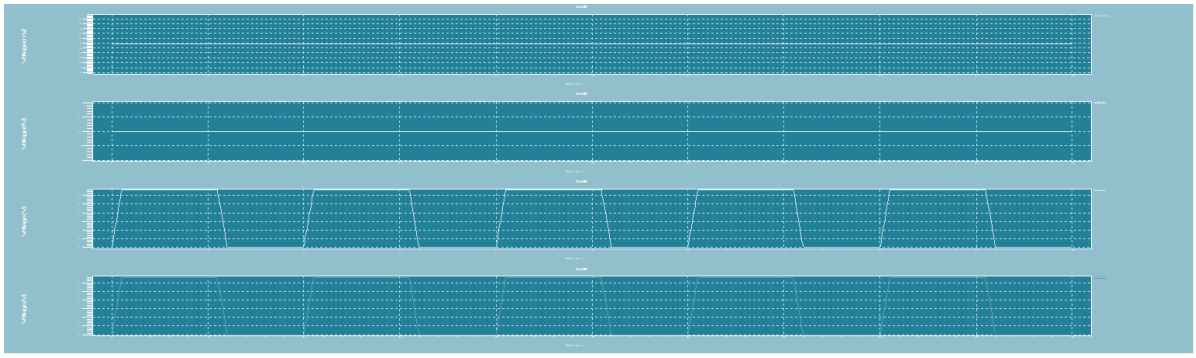

Figure 8 Transient Analysis of Interrupt Controller

5.3 Schematic Diagram of CPU with Interrupt Controller and RAM

The control unit is used to lessen the Interrupt burden of the main CPU and to reduce the required CPU performance,while message buffer RAM is used to store all messages transmitted and received[7].

Figure 9 shows the schematic diagram of CPU with Interrupt Controller And RAM. We have used Tanner Tools for designing this schematic diagram.

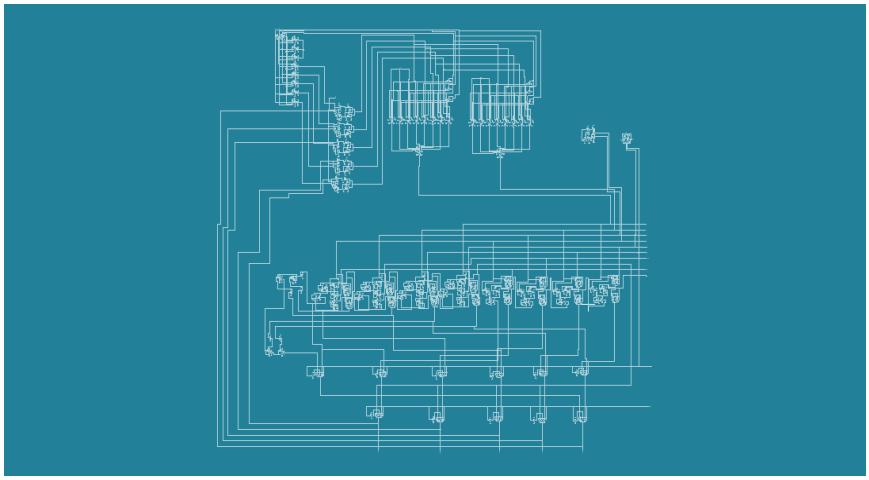

Figure 9 Schematic diagram of CPU with Interrupt Controller and RAM

5.3.1 AC & DC Analysis of CPU with Interrupt Controller and RAM

Transient and DC analysis of CPU with Interrupt Controller and RAM is Shown in **Figure 10** & **Figure 11.**

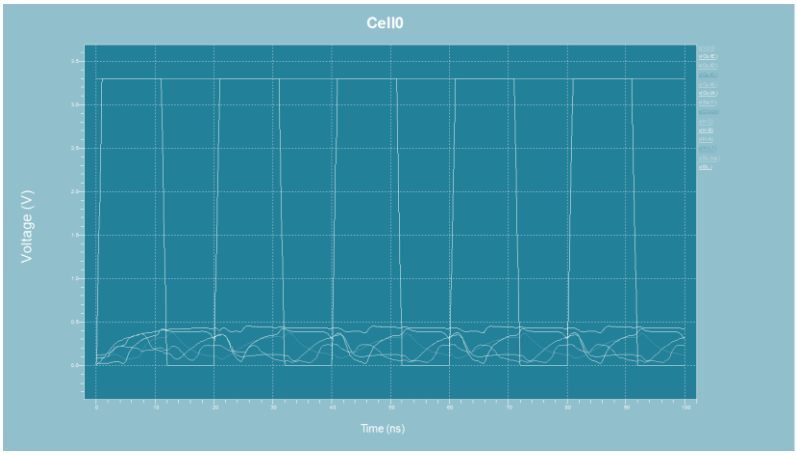

Figure.10 Transient Analysis of CPU with Interrupt Controller and RAM

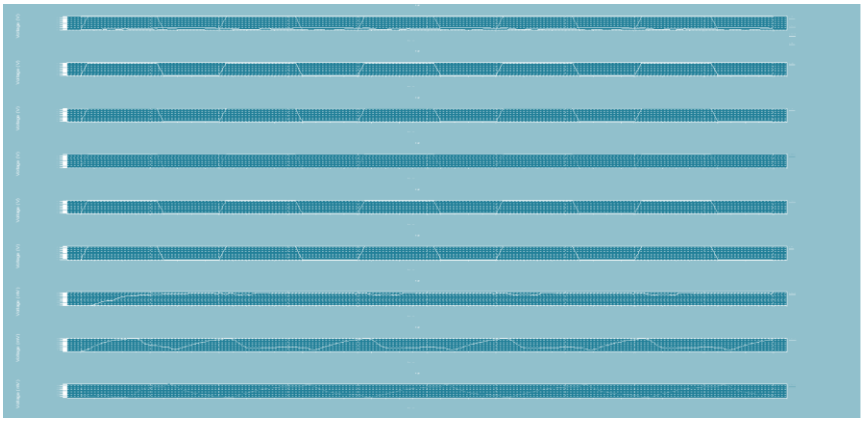

Figure.11 DC Analysis of CPU with Interrupt Controller and RAM

5.4 TIMING REPORT Of ALU

In CPU architecture, ALU of purely combinational ckt, independent multiplier and divider module, Ulti-clocks architecture and hardwired control unit are adopted to get high speed [6,8].

We have generated the timing report of ALU after doing synthesis on Modelsim (SE-5.4a).

a) Clock Information: No clock signal found in this design.

b) Timing Summary: Speed grade=6

c) Minimum Period: No path found.

d) Minimum input arrival time before clock: No path found.

e) Maximum combinational path delay: 61.455 ns.

5.5 TIMING REPORT OF RAM

The timing report of RAM is generated after doing synthesis on Modelsim.

Generated After Place -And-Route

Clock Information

Clock Signal	Clock buffer (FF name)	Load
Clock	BUFGP	1201

Timing summary:

Speed grade: 6

Minimum period: 13.859 ns (Maximum Frequency: 72.155MHz).

Minimum input arrival time before clock: 31.365 ns.

Maximum output required time after clock: 6.788 ns.

Maximum combinational path delay: No path found.

6. Conclusion

We have designed the schematic and layout 8051 microcontroller using tanner tools and studied the transient and DC analysis of 6T based RAM. Interrupt controller of CPU of 8051 microcontroller from timing diagram generated using modelsim (SE-5.4a). Although our effort is focused on creating a new version of the simulator that operates at the machine-cycle or clock-cycle level, the current version operates at the instruction level. Performance will suffer as a result; however, two more enhancements will be made: i) Simulation of Timer 2 and new serial port modes for the 8052 microcontrollers; ii) Detailed simulation of the external bus. Additional enhancements could include the ability to undo and save/load states.

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