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Implementation of Digital Low Dropout Voltage Regulators with low ESR and PSRR

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Abstract: The design of a Digital Low Dropout Voltage Regulators (DLDO) with output voltage is 1.5 V. The load current is in the range of 8 µA to 2 mA with 9% error. The balance of the resistors is an important element in the design of many LDOs, must be taken into account and the ESR tolerances must be determined. The regulator is stabilized with a 1µF output capacitor with 20% tolerance. The temperature range is between -50°C and 100°C for DLDO. The ability of the controller to reject input voltage fluctuations and noise is called PSRR to achieve the large value. The ESR range specified in the specification is between 10m and 300m. In the input voltage range of 1.7V to 2V, the maximum quiescent current under all conditions should be less than 10 µA.

Index Terms—*ESR, PSSR, Transient Response low dropout regulator (LDO).*

I Introduction

The LDO regulator is one of the power supply design elements. This is important for increasing the safety and reducing noise in future transmission lines. This has led to the emergence of architectures called "system-on-chip" architectures (SoCs). This has resulted in the emergence of many different buildings with different needs, using power management systems, DC-DC converters, switching regulators or a combination of these.

The advantage of a linear rectifier is that it can suppress power surges and thus protect noise-sensitive modules, so the "power surge rejection ratio" (PSRR) is a significant constraint of power supplies. An LDO regulator is usually used after a converter, it can handle a higher voltage, but its output can be affected by the surge

Technological LDOs are well suited to provide multiple voltage levels and operate at lower voltages. The LDO can also reduce current consumption to the microampere level in sleep mode.

II DLDO Parameter Analysis

A. Linear Voltage Regulators Fundamentals

The internal resistance of the constant voltage 2.3 should be smaller than the external resistance to ensure that the output voltage remains constant under certain load changes. By adjusting its internal resistance, the voltage regulator maintains a constant voltage according to changes in load.

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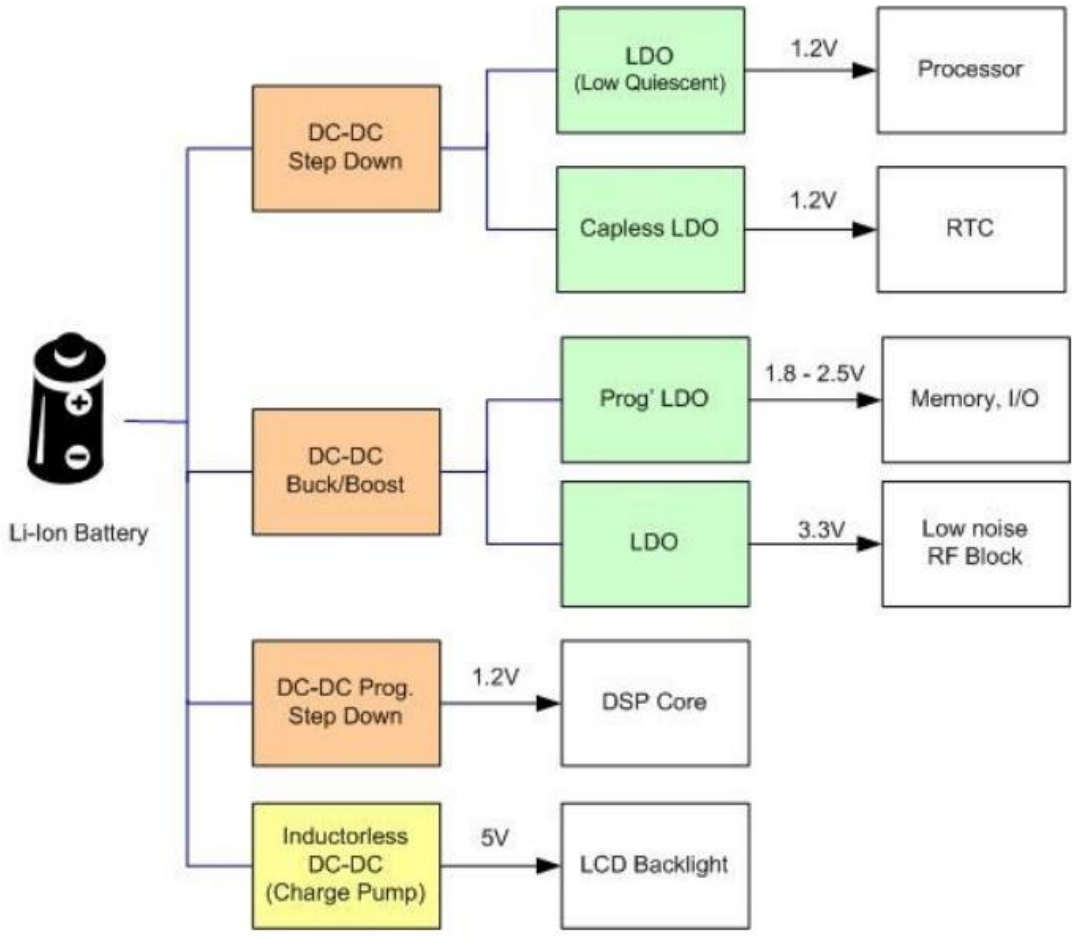

Figure 1: LDO "System on chip" [4]

Apply the voltage divider rule for calculating the "output voltage" of the "voltage source" is :

$$v_{out} = v_{in} \times \frac{r_{load}}{r_{load} + r_{in}}$$

$$= v_{in} \times \frac{1}{1+\frac{r_{in}}{r_{load}}}[v] \ldots\ldots\ldots\ldots\ldots[1]$$

Here

1)$r_{load} = \infty$

This condition represents the "no load"

2)The output voltage maximum = Regulator input voltage.

This condition represents the "Increasing the load causes output voltage to drop from its maximum value" & presents an "output-voltage error" e_{vo}.

This error is defined as a percentage difference between "output voltage under no-load condition" & "output voltage under load condition".

$$e_{vo} = \frac{v_{out-max} - v_{out-load}}{v_{out-max}} \times 100\% \ldots\ldots\ldots\ldots\ldots[2]$$

Where

$v_{out-max}$= v_{out} under no-load condition

$v_{out-load}$= v_{out} under load condition

$v_{out-load}$ & v_{out} can be replaced with v_{in} put the value in equation 1.

So the voltage error in the form of the resistor ratio ia r_{in}& r_{load} :

$$e_{vo} = \frac{r_{in}}{r_{in}+r_{load}} \times 100\% \text{.....[3]}$$

So conclusion from equation 3 is decreasing load resistance r_{load} if voltage error e_{vo} is increasing.

By using the feedback circuits this error to be minimized. Here regulates a variable internal resistor and changes in the load for maintaining a constant ratio of "internal-resistance" to "load resistance":

$$\frac{r_{in}}{r_{load}} = k$$

$$r_{in} = r_{load} \times k\Omega \text{.....[4]}$$

From this equations we get the linear output of r_{in} & r_{load}.

B. Temperature Considerations

To ensure that the junction temperature is within the limits, the maximum allowable loss PD (max) and the actual loss PD are calculated; the latter must be less than or equal to PD (max). To protect the device and ensure the integrity of the components, the maximum junction temperature must not exceed 125°C. Thermal shutdown shuts down the device if the temperature exceeds 150°C. This limit limits the amount of power dissipation the controller can handle in any given application.

To make certain that the junction temperature is in the limits, the maximum allowable loss PD (max) and the real loss PD are calculated; the latter have to be less than or equal to PD (max). To defend the tool and ensure the reliability of the components, the maximum junction temperature should no longer exceed 125°C. Thermal shutdown shuts down the tool if the temperature exceeds 150°C. This restriction limits the quantity of electricity dissipation the controller can handle in any given software.

The most electricity dissipation limit is determined with the aid of the subsequent formula.

$$P_{d(max)} = \frac{t_{jmax} - t_a}{R_{\theta ja}}$$

where

t_{jmax}=Junction temperature[℃] maximum

$R_{\theta ja}$=Junction to ambient thermal resistance

t_a=Ambient temperature

The regulator dissipation is

$$p_d = (v_{in} - v_{out}) \times i_{out}$$

C.ESR and Transient Response

LDOs regularly require outside output currents to be strong. In speedy-reaction programs, capacitors are used to guide the burden modern-day whilst the LDO amplifier is responding. in many applications, one capacitor is used to help both features. Impedances are both resistive and inductive. The resistive impedance is known as the equal series resistance (ESR), and the

inductive impedance is known as the equivalent collection inductance (ESL).

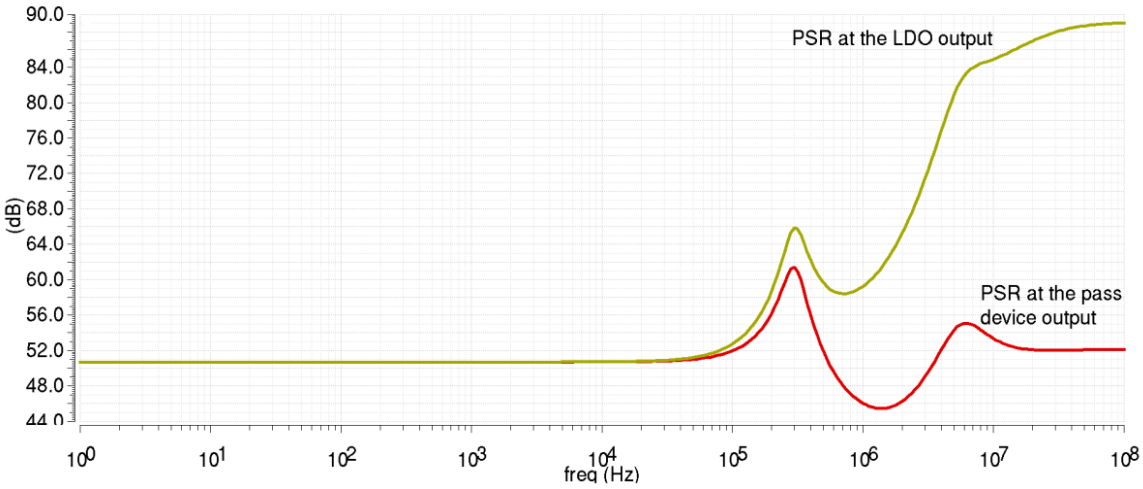

Figure 2: LDO regulator output PSSR

D. Power Supply Ripple Rejection

Another important factor in AC power supply is the "Power Supply Ripple Rejection or PSR" (power supply short circuit resistance). As we know, it defines the ability of the regulator to accept input voltage variations above a certain frequency.

As usual, as shown in Figure 2, we will see that the PSR amplitude decreases around the increasing convergence bandwidth used satisfactory value of 51 dB.

III Result and discussion

A. Transient Analysis

We simulated the periodic analysis and evaluates the real-time behavior of the circuit as it changes the signal size. The system has large levels of low load current, the transition from maximum to minimum.

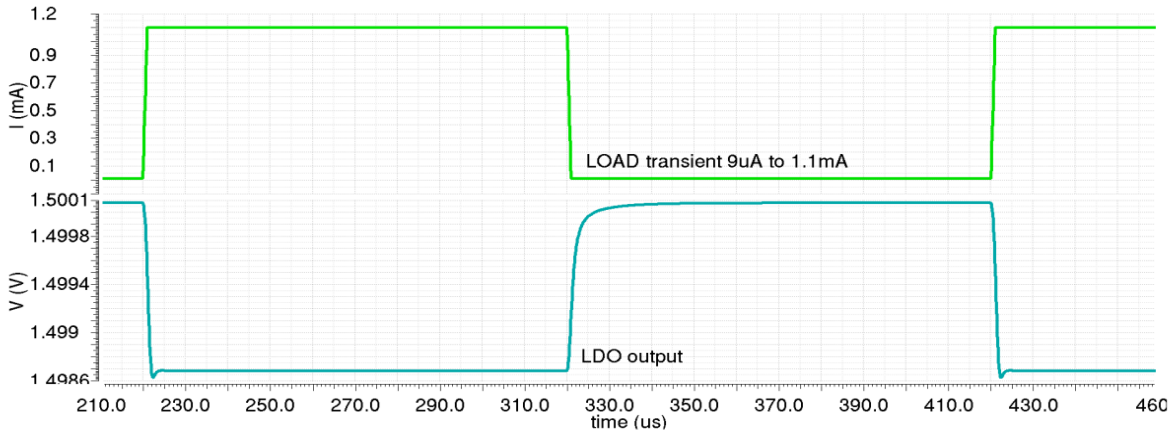

Figure 3: Response of Load transient

At a low frequency of 5 kHz, the load current changes from 9 µA to 1.1 mA is shown in the figure 3 as a consequence growing a voltage drop throughout the capacitor. The ESR isn't very large and the load current is small like millivolt range, which is acceptable.

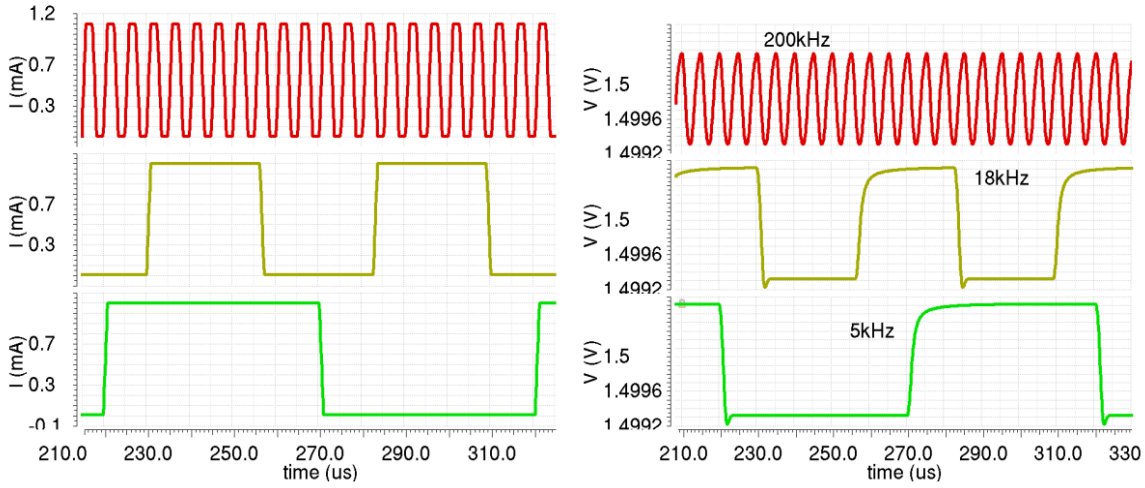

Figure 4: Load transient for 5kHz, 18kHz and 200kHz

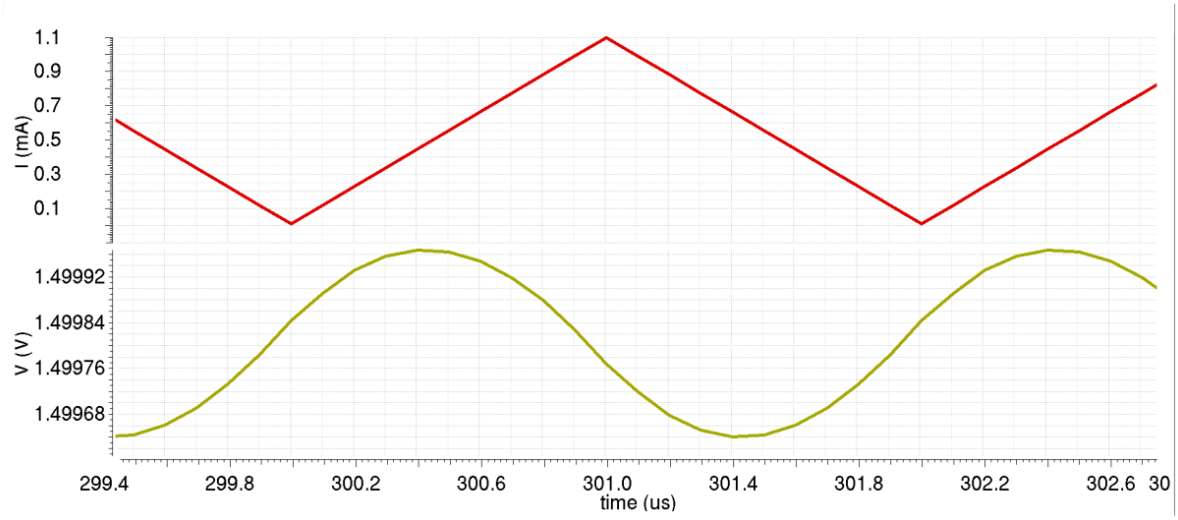

Figure 5: Load transient for 1MHz

In figure 5 shows that the output is unstable during frequency change. The gain of the system decreases to the change in output.

B. Line Transient

Line transients behave differently than load transients. The difference in steady-state voltage for line transients is much smaller than the difference for supply rejection and line regulation. We can also see that the overshoot is in the direction of load transient overshoot. Also, line transients under small load current are very different from line transients under large load current as shown in the figure 6 & figure 7.

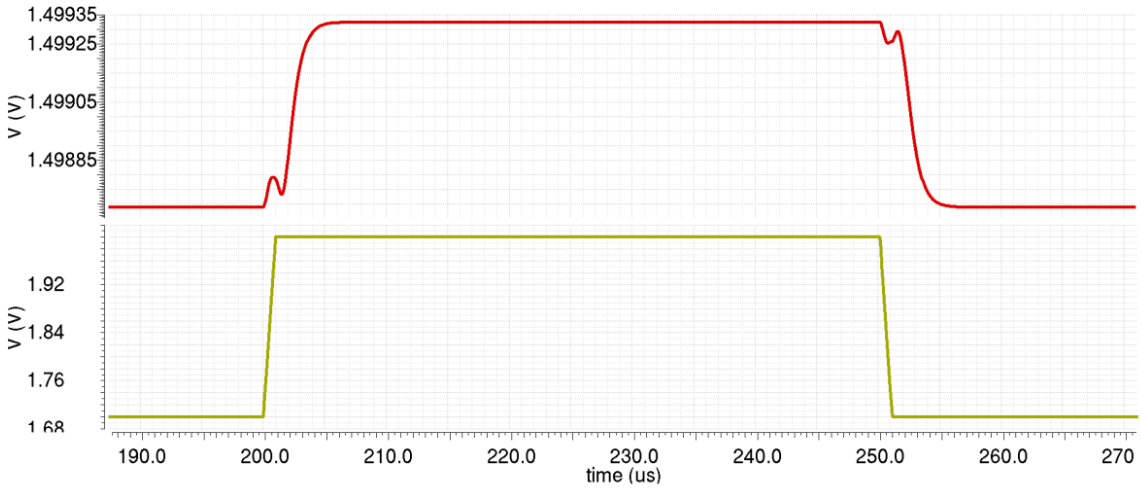

Figure 6: Line transient response with load current

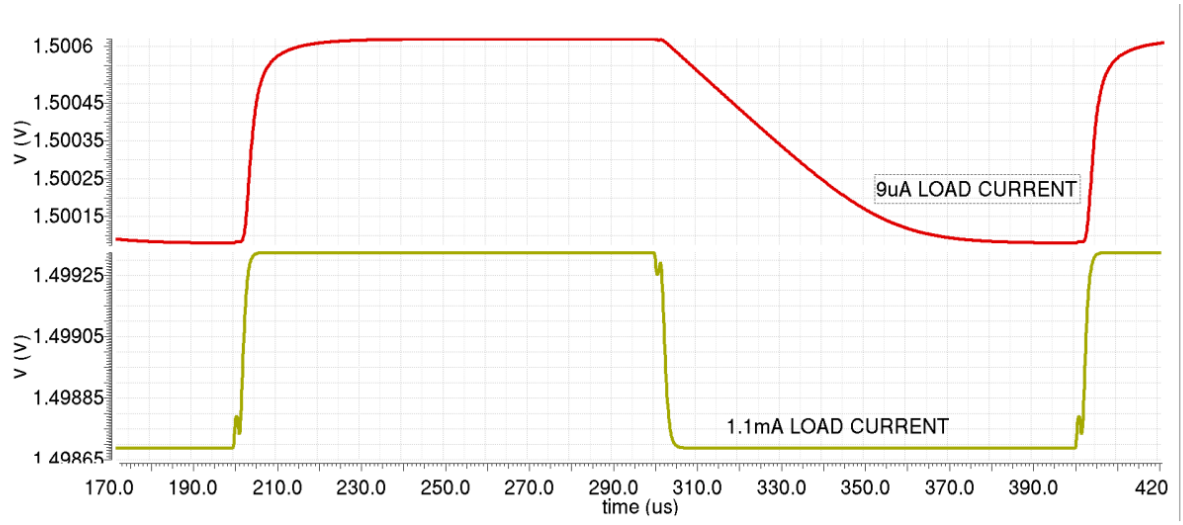

Figure 7: Line transient response with load current maximum.

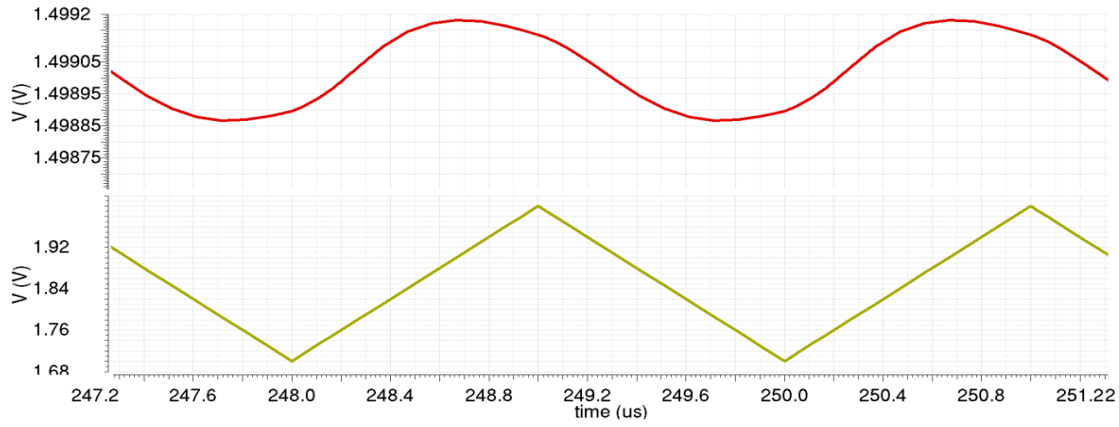

Figure 8: Line transient response with load current higher frequency

it is only charged by the supply current because it has been discharged by a small load current of about 15 µA. This can be seen in Figure 8.

For a small load current.

1) voltage = high, Response = fast, capacitor = charged (by current from the supply).
2) voltage =drops,output capacitor =retains charge for a very long time (only charged supply current).

C. Power Ripple Suppression

A very simple time-varying measurement of the PSR. The output ripple to the input ripple have the same PSR. V_{IN} supply line have transient ripple signal .

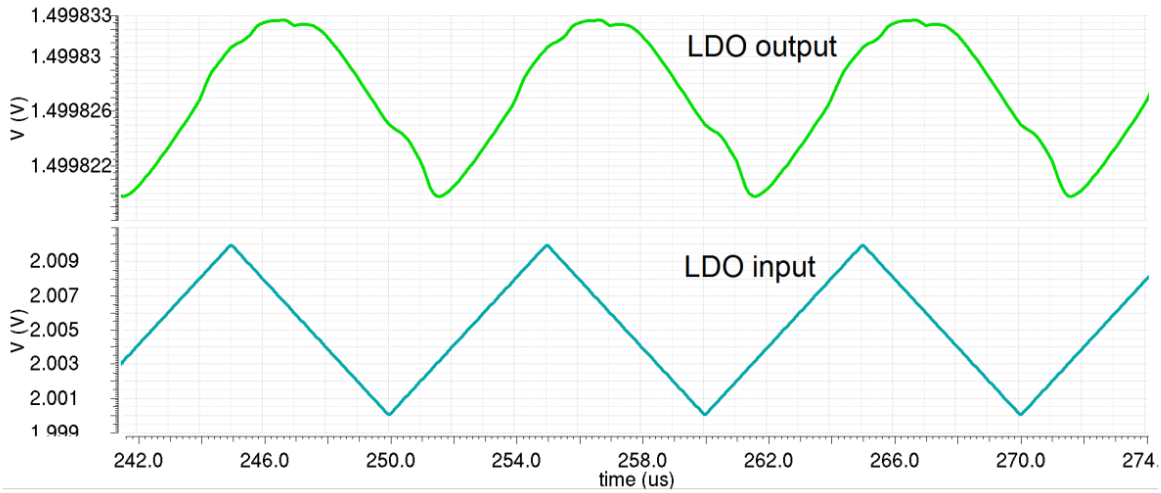

Figure 9: Transient response with power supply ripple of 12 mV

When a 12 mV ripple is added to the power line, we can see the change among the "output" and the "input" voltage. The output varies in the microvolt range.

The total PSR is the "total change in input voltage" & "total change in output voltage" is

$$PSR = \Delta vin\ \Delta vout$$

Giving a PSR of about 51 dB, depending on frequency.The output changes with temperature is useful.

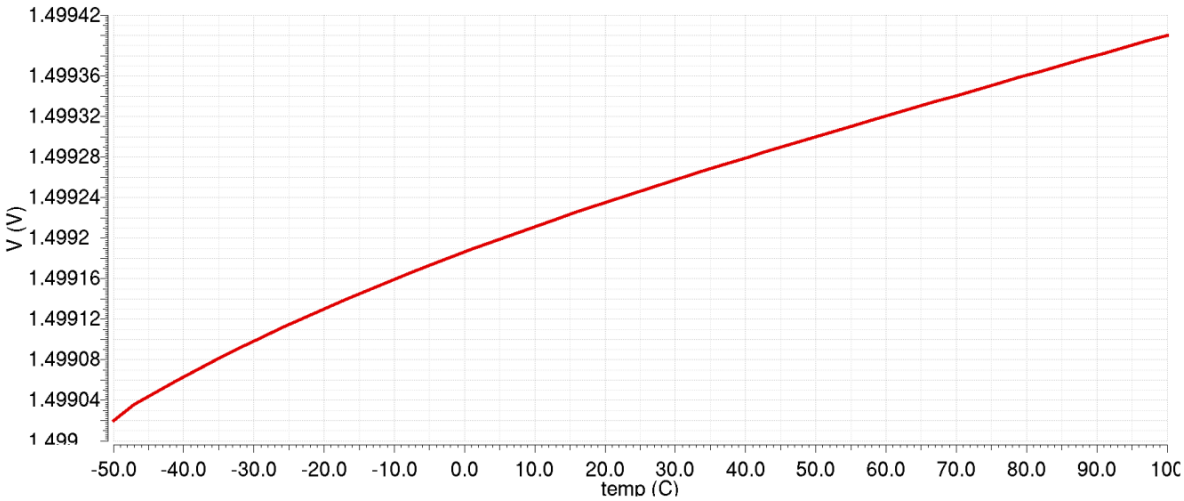

Figure 10: Output voltage variation with temperature

IV Conclusion

The undersigned LDO regulator was measured using a simulator in the "Cadence design environment". It is important to design a stable LDO regulator across all process and parameter aspects. "Low output current" is balanced with "low quiescent current" and "low power loss". The Efficiency ranges from 78% to 89% and it is depending on input voltage. The final design is based on specifications, but there is still a lot of room for improvement. Bias strategies for load current can be used to increase the stability of power supplies while ensuring consistent circuit performance. To minimize output voltage, drop, the capacitor should have "low ESR". For the LDO response time, minimum voltage required to support.

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