International Journal of
INTELLIGENT SYSTEMS AND APPLICATIONS IN ENGINEERING
ISSN:2147-6799 www.ijisae.org Original Research Paper

Performance Analysis of Circuit Routing Using Monte Carlo Tree Search

Deepmala Sharma[1], Jitendra Ahir[2] and Laxmi Singh[3]

Submitted: 05/09/2024 **Revised:** 22/10/2024 **Accepted:** 01/11/2024

Abstract: This paper uses a PCB routing approach using Monte Carlo Tree Search (MCTS)-based global routing. Routing plays a very important role in the design of printed circuit boards (PCBs). Configure the partition for the routing solution. The router shows experimental results with wirelengeh optimization. The proposed technique reduces the overlap problem between global and detailed routing. Improved MCTS algorithm improves Search efficiency, reducing blocking of routed nets to inconsistent networks.

Index Terms*: Global routing, Monte Carlo tree search, Printed circuit board*

I. Introduction

Routing is a key feature in the design process of printed circuit boards (PCBs) as strategic metal wires are strategically placed to establish connections between pencils and maintain predefined design rules. It's the step [1]. Currently, automated routing methods usually approach the problem based on two different stages: escape routing and surface routing handle it independently [2] [3]. Escape Routing [4] focuses primarily on determining the optimal path within the boundaries of a particular device, such as BGA devices (ball grid arrays). Surface Routing [5], on the other hand, deals with determining routes between locations at the boundaries of various devices on a circuit board. However, the independent treatment of these two routing stadiums leads to unique topics. In some cases, reaching the success of an escape routing solution will inadvertently render surface routing impossible [3]. Existing escape and surface routing approaches demonstrate the effectiveness of handling devices packed into ball grid arrays (BGAs) [4], but difficulties arise when in non-BGA PCB designs [2]. Such limitations underscore the need for a more cohesive and comprehensive routing approach that can meet a wider range of PCB configurations and components. Inspired by the global, detailed routing approach of Integrated Circuit (IC) design [6], we propose a global, detailed routing strategy focusing on new pads tailored to PCBs. Our approach involves systematic division of the roofer area of polygon tiles based on the location and dimensions of individual pads, regardless of their association with the particular component. At the global routing level, NET sequences of polygon tiles are assigned, and at the detailed routing level, these polygon assignments are translated into polylines that form the wires. By directly fighting pad-to-pad routing, our method optimizes paths that are agnostic for devices of pathing types, and effects the decoupling problems that plague traditional escape and surface routing methods. It will ease the situation. Dynamically splits polygon tiles when assigned to paths in the global routing phase to ensure seamless consistency between global routing and detailed routing properties. This approach ensures that if a detailed routing solution for this path leads to an intersection within this particular tile, no polygons are assigned to two paths.

1Ph.D. Scholar, Department of Electronics & Communication Engineering, Rabindranath Tagore University (RNTU), Bhopal

2,3Professor, Department of Electronics & Communication Engineering, Rabindranath Tagore University (RNTU), Bhopal

sharmadeepmala85@gmail.com,

Jitendra.ahir@aisectuniversity.ac.in,

laxmi.singh@aisectuniversity.ac.in

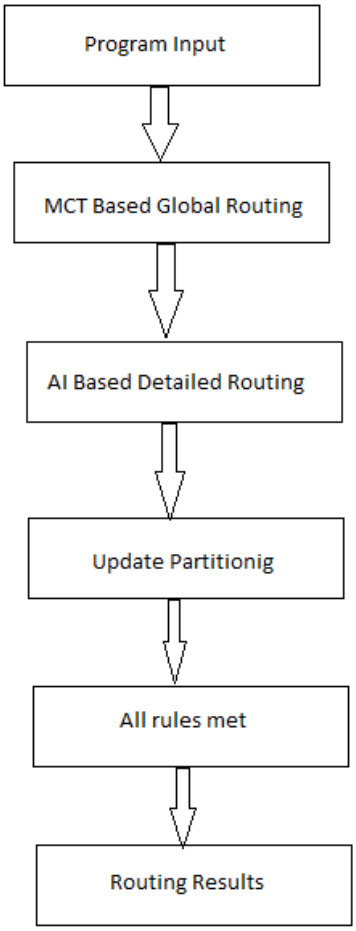

Fig. 1: Structure of Proposed work

First, circuit routing problems for PCB and VLSI designs are defined and traditional routing-algorithms is introduced. Furthermore, we consider the study of routing algorithms using MCTS to improve routing performance. Second, routing studies are analyzed with AI. Compared to traditional routing methods, AI technology allows circuit algorithms to be more flexible to solve a variety of placement and routing problems. AI-based circuit development technologies can improve performance by repeatedly optimizing component placement and routing processes. Analyze the characteristics of AI technologies used in circuit design. Additionally, routing methods have been introduced, using state-of-the-art AI technology using AI technology (DRL) in Deep Construction Learning (DRL). DRL can act as a manufacturer of the best choice decisions in a variety of dynamic problems. Therefore, it is used in a variety of research fields such as communication systems, parameter control, and circuit design automation. Third, this paper analyzes the challenges and considerations of AI-based routing algorithms. AI-based enhanced routing technology is also presented to improve routing performance.

II. Monte Carlo Tree Search (MCTS)

Although an MCT-based approach was used when circuit routing problems occurred [1] [2], MCTS was used especially for the global routing stage where search space was low compared to overall routing problems. This allows for efficient solution of complex circuits in a short amount of time [9].

MCTS repeatedly expands the search tree node with the node until the maximum number of iterations is reached. Each iteration consists of four next stages [20].

Selection

- Recursively select a fully-expanded child in the search tree Starting from the root node, until reaching a non-fully expanded node or a node representing a terminal state as shown in the selection part.
- If all its potential children are added to the search tree a node is fully expanded. Otherwise, the node is non-fully expanded.

Expansion

By adding a new node expanding the search tree as a child of a non-fully expanded node selected in the selection step.

Rollout/Simulation

Acting over all remaining unexpanded decisions until reaching the terminal state Starting from the newly expanded node and following a fixed strategy.

Backpropagation

Sample the incentive and apprise all the tree nodes that have been traversed, when the rollout reaches the terminal state.

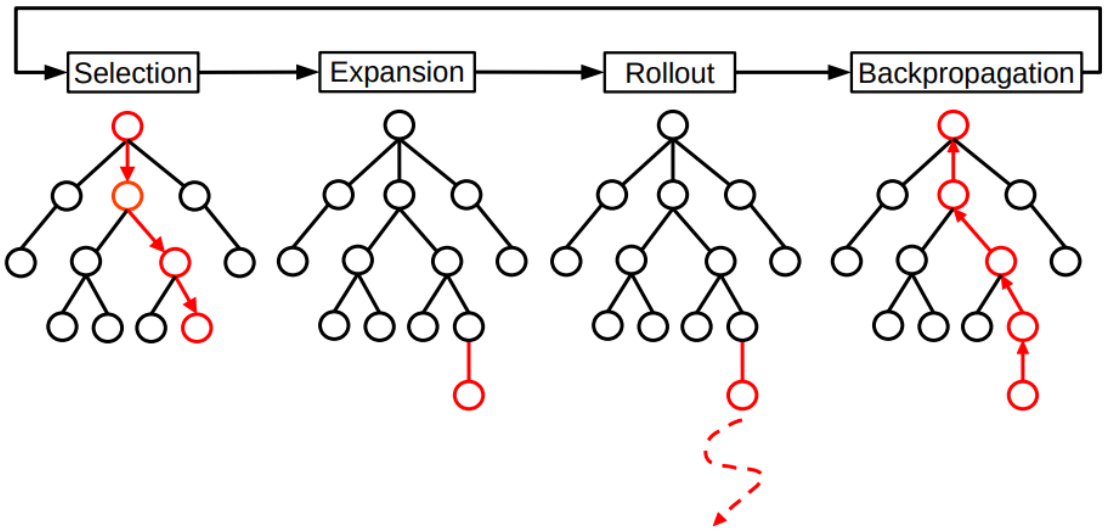

Fig 2: Stages of the "Monte Carlo Tree Search"

Global Routing And Detailed Routing

Global routing and detailed routing are two general steps of the IC routing [1]. Global Routing distributes routable areas and creates graphical presentations. Global Routing provides paths for all networks and describes the sequence of partitions that traverse the network. Detailed routing converts partition allocations to polylines. The traditional two-stage approach may have insufficient coupling between global routing and detailed routing [8], which may lead to an invalid detailed routing solution. there is. To address this issue, our approach involves dynamic partitioning, which divides partitions occupied by detailed routing cables. This ensures that non-broadcast networks do not exceed the solution wire and release coupling issues.

Pcb Routing

PCB routing is becoming increasingly tough and time-consuming due to the continuous increase in pind density and routing layers. Traditionally, PCB routing was addressed in two phases: escape trout and surface routing [4]. Escape routing focuses on determining path restrictions for component pencils (e.g. BGA devices), whereas surface routing sets paths between device boundaries [2]. Simultaneous escape routing (SER). The UER and OER include routing within the BGA without PIN order limits along the BGA boundary. The SER deals with escape routing for two

BGAs and requires a consistent order from the escape route. Previous research has proposed various methods.

Surface routing focuses on solutions to routing problems with length adjustment limits. It was proposed to tackle this issue. For example, [3] proposed a complete PCB routing approach, including SER, later reinforcement, and routing of gridless areas. However, routing using non-BGA is not considered. [2] proposed a one-time PCB routing mechanism with a complete board based on the algorithm. PCB routing using non-BGA packages was considered in the work. However, although algorithms usually do not find a suboptimal solution or find a solution, some networks are in a continuous manner, as wires in the early routing nets can make later networks insoluble. It is connected.

III. Methodology And Results

Figure 2 illustrates a routing approach. The main routing formula leads all networks. It includes layer-conscious partitioning and graphics structure. Your design statistics will be presented. The net order used in our approach is the standard order provided by all PCB designs. In particular, our approach successfully guided all the test PCBs, but the free routing and deep-PCBs do not forward two PCBs. When it comes to optimizing wire length, our approach has surpassed the comparative router to reach the shortest overall cable. However, regarding this term, our approach required more time in most test cases than free routing and algorithms in [2].

It is important to note that our approach generates more generation compared to free routing. This is due to prioritization of the routing algorithm as a key consideration, followed by wire length optimization. To achieve this, we included specific mechanisms in global and detailed routers to reduce blocking of routes of routed nets to unequipped networks. These mechanisms include splitting and reward design of MCTS-based global routers, and regularization of the routers they are brought into. The combination of these mechanisms allowed us to successfully guide all test PCBs and optimize both in scope and lucidity at the same time.

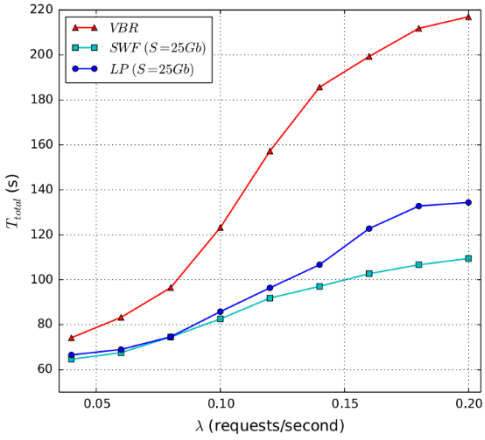

Fig. 3: Ttotal versus λ

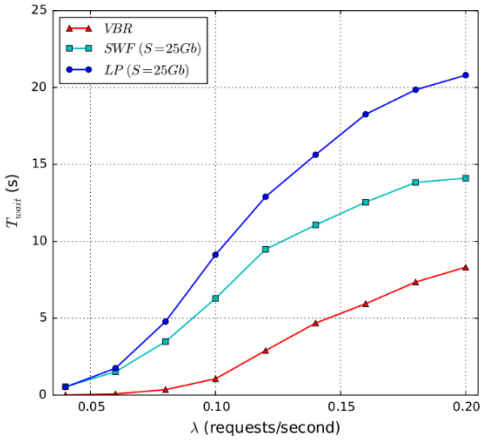

Fig. 4: Twait versus λ.

Fig. 3 and fig. 4 shows that the circuit routing performance differs based on performance. The size is determined as 25 GB as shown in the diagram fig. 3 and fig. 4. Use a small range to send data for bandwidth. Here, data transfer times and long delays are significantly reduced as data transmissions can occur at the switching nodes latency. The performance of the low arithmetic complexity of these algorithms is efficient.

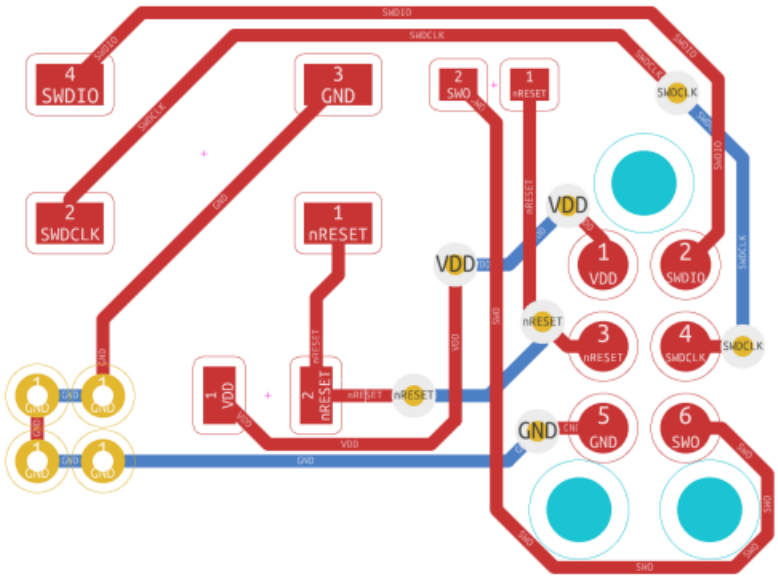

Fig. 5: Routing result for the PCB design

IV. Conclusion

An effective routing strategy is one of the ways to achieve the goal. Networks are analyzed from local and global perspectives of or nearby centrality. The results demonstrate that our strategy reduces the load distribution rather than reduce the overall burden on the network. Finally, consistent results are achieved through simulation results. This is a strategy that presents a PCB.

References

[1] K. Li, X. F. Gong, S. G. Guan, and C.-H. Lai, "Analysis of traffic flow on complex networks," Int. J. Mod. Phys. B, vol. 25, no. 10, pp. 1419–1428 ,2012.

[2] X. Gao et al., "Global hybrid routing for scale-free networks," IEEE Access, vol. 7, pp. 19782–19791, 2019.

[3] X. P. Wang, G. Yu, and H. T. Lu, "A local information-based routing strategy on the scale-free network," Mod. Phys. Lett. B, vol. 23 , no. 10, pp. 1291–1301, 2009.

[4] G. Liu and Y. S. Li, "Routing strategy for complex networks based on gravitation field theory," Acta Physica Sinica, vol. 61, no. 24, 2012, Art. no. 248901.

[5] G. Liu and Y.-S. Li, "Study on the congestion phenomena in complex network based on gravity constraint," Acta Physica Sinica, vol. 61, no. 10, 2012, Art. no. 108901.pp. 1717–1730, Sep. 2019.

[6] M. Pan and C. Chu, "IPR: An integrated placement and routing algorithm," in Proc. ACM/IEEE Des. Autom. Conf., 2007, pp. 59–62.

[7] K.-R. Dai, C.-H. Lu, and Y.-L. Li, "GRPlacer: Improving routability and wire-length of global routing with circuit replacement," in IEEE/ACM Int. Conf. Comput.-Aided Des. Dig. Tech., 2009, pp. 351–356.

[8] X. He, W.-K. Chow, and E. F. Y. Young, "SRP: Simultaneous routing and placement for congestion refinement," in Proc. ACM Int. Symp. Phys. Des., 2013, pp. 108–113.

[9] W.-H. Liu, C.-K. Koh, and Y.-L. Li, "Optimization of placement solutions for routability," in Proc. ACM/IEEE Des. Autom. Conf., 2013, pp. 1–9.

[10] T. A. Fontana et al., "ILP-based global routing optimization with cell movements," in Proc. IEEE Comput. Soc. Annu. Symp. VLSI (ISVLSI), 2021, pp. 25–30.