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Development Of A 33 Ghz Low Noise Amplifier Utilizing The Multigate Technique For Cascode Devices

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Abstract

The presence of increased parasitic components in silicon-based nanometer (nm) scale active devices results in various performance trade-offs when optimizing key parameters, such as maximum frequency of oscillation (fmax), gate resistance, and capacitance, among others. A common-source cascode device is frequently employed in amplifier designs operating at RF/millimeter-wave (mmWave) frequencies. Besides intrinsic parasitic components, extrinsic components arising from wiring and layout effects are also vital for the performance and precise modeling of these devices. This study presents a comparison of two distinct layout techniques for cascode devices aimed at optimizing extrinsic parasitic elements, including gate resistance. A multi-gate or multi-port layout technique has been proposed to optimize gate resistance (rg). Measurement results indicate a 10% reduction in rg for the multi-gate layout technique when compared to a conventional gate-above-device layout for cascode devices. Nevertheless, the conventional layout demonstrates smaller gate-to-source and gate-to-drain capacitances, resulting in enhanced performance regarding speed, specifically fmax. An LNA has been designed to operate at a frequency of 33 GHz utilizing the proposed multi-gate cascode device. The LNA achieves a measured peak gain of 10.2 dB and a noise figure of 4.2 dB at 33 GHz. All structures have been designed and fabricated using 45 nm CMOS silicon on insulator (SOI) technolog.

Keywords mm-wave · RF · LNA · Receiver · 5G · Multi-gate · Communication systems · CMOS · SOI

1 Introduction

Current wireless communication technologies are unable to meet the growing data rate demands from wireless networks, which stem from the rising number of multimedia applications and devices. To satisfy the capacity requirements of next-generation networks, more sophisticated and higher-order modulation techniques, such as quadrature amplitude modulation (QAM), are essential. This also necessitates higher signal-to-noise ratio (SNR) values for the radio frequency front end (RF FE) modules. The limited availability of sufficient bandwidth (BW) in existing systems poses a significant challenge mobile communication technologies, utilization of unused mmWave frequency bands for fifth generation mobile communication (5G) is needed. Third generation partner- ship project (3GPP) has standardized the first frequency bands for 5G new radio (5GNR) from 24 to 29 GHz and 39 GHz. Different 5GNR frequency bands with available BW are listed in Table 1.

Moving to mmWave communication also leads to lots of challenges in terms of path loss, scalability, packaging and its associated parasitic effects. Due to that phased arrays are used to increase the antenna aperture in order to com- pensate free space path loss at mmWave frequencies [2]. Miniaturization of bigger antenna systems is realized using silicon based technologies (CMOS and BiCMOS) which offer integrated solutions for faster and scalable mm Wave systems for phased arrays [3]. Applications of silicon-based technologies are classified by the performance of their active devices and passive structures. For example, nanoscale bulk CMOS technologies offer ultra-fast tran- sistors which are useful for logic or digital circuitry. However, they have low ohmic substrate which results in

Table 1 Allocated millimeter-wave frequency bands in 5G NR FR2 standard [1]

5G NR FR2 bands	Frequency (GHz)	Bandwidth (GHz)
n257	28	3
n258	26	3.250
n260	33	3

In passive structures, there is a notable increase in losses. Conversely, in conjunction with ultra-fast transistors, CMOS silicon-on-insulator (SOI) technology provides the potential to leverage high resistive substrates for the integration of high-performance passive structures. Additionally, SOI technology alleviates substrate-related cross-talk and enhances isolation in metal oxide semiconductor (MOS) based switches. Consequently, CMOS SOI technology is recognized as a promising candidate for future mmWave integrated systems that combine RF front ends and digital baseband circuitry on a single chip. The gate length of a transistor is viewed as a fundamental driving factor in the scaling of technology. The high-frequency performance of a transistor is determined by the gate length and its related parasitic components, such as capacitance and resistance. The characteristics of these parasitic components are greatly influenced by the layout design. For instance, rather than utilizing a single side connection, the gate resistance (rg) of a multi-finger device can be significantly decreased through dual side connections of the poly silicon gate finger to metal 1 (M1) [4]. Cutting-edge silicon technologies provide scalable intrinsic models for transistors that incorporate realistic parasitic components across several metal layers (e.g., M3). Nevertheless, signals at mmWave frequencies are preferably routed on the upper metal layers due to their lower metal resistance, which requires the extension of device terminals from lower to higher metal layers. The modeling of these interconnects' forms part of the device's extrinsic model and depends on the layout strategies employed by the designer. These parasitic effects, both intrinsic and extrinsic, are integral to defining the maximum oscillation frequency of the device, denoted as fmax, and expressed as,

$$f_{max} = \frac{1}{4\pi}\sqrt{\frac{g_m}{r_g C_{gd}(C_{gs}+C_{gd})}}, \quad (1)$$

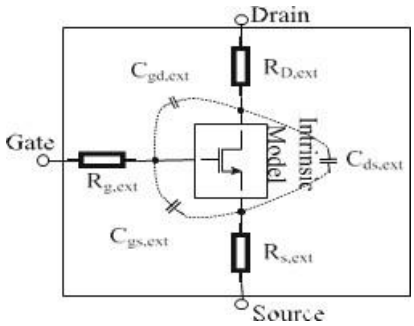


Fig. 1 Extrinsic components of an NMOS transistor

The additional wiring in the traditional layout style introduces extra parasitic components at this node. To compensate for this parasitic capacitance at mmWave operational frequencies, additional inductance is utilized to enhance interstage matching [5]. Nevertheless, these parasitic components can be significantly minimized by eliminating the extra wiring at the junction and optimizing the active area [6, 7].This document serves as an extension of our prior research presented in [8]. Within this paper, two distinct layout styles are developed, characterized, and compared based on key performance parameters. Section 2 outlines the layout design for cascode devices. Section 3 discusses design techniques pertinent to mmWave IC designs, including ground plane considerations and port definitions in electromagnetic (EM) simulation tools, among others. A 33 GHz LNA is designed utilizing a multi-gate device and is detailed in Section 3. The experimental results pertaining to device characterization and the LNA are examined in Section 4. The conclusions of this paper are provided in Section 5

2 Cascode devices

In addition to intrinsic parasitic components, interconnects between devices add additional parasitic effects in the modelling of active devices. These parasitic components are part of the extrinsic model of the device mainly due to intrinsic and extrinsic model

due to wiring and therefore, they should be characterized carefully for optimum device performance. Silicon foundries provide intrinsic models of active devices which include the parasitic effects from extension of device terminals upto few metal layers. However, further extension of these terminals upto signal routing layer is custom made and these extensions are modeled in extraction tools (e.g. EM or RC extraction)the metal wiring and via connections as shown in Fig. 1.

Certainly, the device behaviour is dependent on both

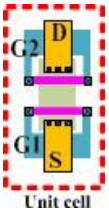
where g_m is the transconductance of the device and

depends on the current density of the technology, C_{gs} and C_{gd} are the parasitic capacitance at gate terminal. Cascode devices are largely used in amplifier designs due to their benefits of better gain and improved stability conditions. Aforementioned modelling approach of a single device can also be applicable to characterize the CS stage with cas- code device and it can be treated as a three terminal device as shown in Fig. 1. The junction between two devices adds

2.1 Optimization of r_g or f_{max}

The additional wiring in the traditional layout style introduces extra parasitic components at this node. To compensate for this parasitic capacitance at mmWave operational frequencies, additional inductance is utilized to enhance interstage matching [5]. Nevertheless, these parasitic components can be significantly minimized by eliminating the extra wiring at the junction and optimizing the active area [6, 7].This document serves as an extension of our prior research presented in [8]. Within this paper, two distinct layout styles are developed, characterized, and compared based on key performance parameters. Section 2 outlines the layout design for cascode devices. Section 3 discusses design techniques pertinent to mmWave IC designs, including ground plane considerations and port definitions in electromagnetic (EM) simulation tools, among others. A 33 GHz LNA is designed utilizing a multi-gate device and is detailed in Section 3. The experimental results pertaining to device characterization and the LNA are examined in Section 4. The conclusions of this paper are provided in Section 5.

Nevertheless, the capacitances associated with these junctions can be considerably diminished by eliminating the metal wiring within the junction and by sharing the active area between the two devices configured in cascode. The multigate technique for stacked devices, as proposed in [6], represents one viable approach to minimizing inter-stage wiring parasitics. This study presents a design and comparison of two layout techniques for cascode devices, namely the conventional style and the multi-gate style. The proposed multi-gate style layout contributes to the reduction of inter-stage wiring, as elaborated in [6], and facilitates a greater number of metal M1-to-M5 vias being implemented within the same device area when compared to the conventional layout. This increased quantity of metal M1–M5 vias aids in further decreasing rvia,ext as indicated in Eq. 2.



$$R_{g,tot} = R_h + R_v + r_{via,int} + r_{via,ext} + r_{wire} \quad (2)$$

where R_h and R_v are horizontal and vertical resistance of a

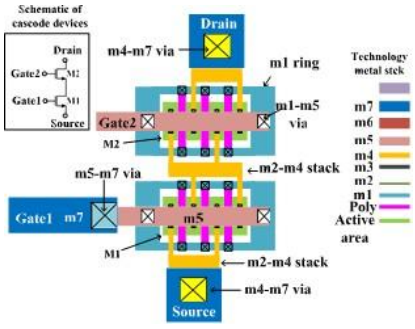


Fig. 2 Conventional-style schematic and layout of cascode devices

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layout style having 20 gate fingers is selected for comparison.

2.2 Conventional style layout

Figure 2 shows a conventional gate-above-device layout style of a cascode device [4]. Two transistors are placed in a vertical orientation on top of each other. To reduce $R_{g,int}$ of transistors, gate fingers are double connected from two sides using a ring of metal M1. Input signal from a ground- signal-ground (GSG) pad is routed at metal M7 and brought to M5 Near the gate of the common-source device M1, which is routed over the transistor and connected to the gate ring at metal M1 from both sides in the horizontal direction, as illustrated in Fig. 2.To ensure sufficient current handling capability of the metal wires, the source and drain connections of each finger are elevated to metal layers M2 to M4 and interconnected with a broader stack of metal layers spanning M2 to M4. These connections are further extended and linked to the thick metal layer M7. This additional extension of the drain and source connections aids in minimizing the extra capacitive coupling caused by the thick metal lines between various nodes, for instance, the shared area of the gate at M1 enhances the quantity of vias at the gate terminal. The gate signal is directed through metal M5 from the top of the structure and is connected to the gate contacts via these M1–M5 vias.. As depicted in Fig. 3(b), there are at least four times as many M1-to-M5 vias compared to the structure shown in Fig. 2, which serves to reduce rvia,ext. Additionally, the wiring resistance is reduced by half by routing the gate signal through metal M5 in two parallel branches, which aids in decreasing the rwire. The layout presented in Fig. 3(b) is effective for optimizing rg,ext. However, this comes with the consequence of increasedcgg = cgd + cgs.

2.3 Multi-gate style layout

The multi-gate layout technique is designed by utilizing the active area of two transistors to remove the need for intermediate metal contacts between the drain and source terminals of the transistors used in cascode devices [6, 7]. Illustrated in Fig. 3(a) is a unit cell featuring a 1um finger width that employs the multi-gate technique. Each cell incorporates a double connected gate finger at metal M1. The source and drain connections are further extended from the device through a stack of metals M2–M4. A distribution network comprising such cells is arranged vertically, allowing the gate connection at metal M1 to be shared between two cells. Additionally, a via from M1 to M5 is positioned within this lay manufacturing processing [11]. Moreover, eddy currents can be induced in this solid metal plate resulting in sub- stantial loss in passive devices at mmWave frequencies. Contrarily, a local ground plane can be used as an RF ground reference which provides local reference for the excitation ports as shown in Fig. 4(b). Generally, a ground plane is composed of thick metal layer from the available metal stack of the technology due to their lower sheet resistance. Alternatively, multiple metal layers are stacked together to realize low impedance metal ground plane.

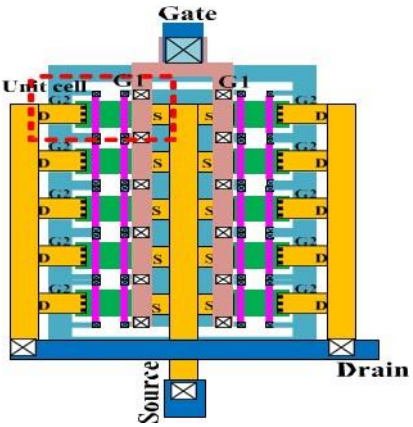


Fig 4

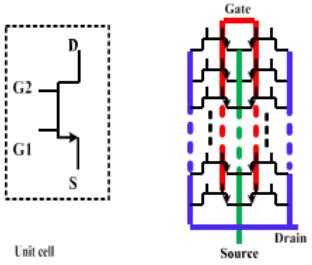


Fig 3

In bulk CMOS process, low resistive substrate requires metal ring (guard ring) connected with the metal ground plane around active and passive devices in order to offer low ohmic paths for currents induced from substrate cou- pling to reduce cross talks between neighbouring devices. In such case, a wall of ground plane around passive devices consisting of all metal layers is used which offers addi- tional benefits of isolation between neighbouring devices. However, in high-resistive substrates, e.g. CMOS SOI, substrate connections (guard ring) are not necessary around passive devices and therefore, a metal ground plane at top metal layer with enough current handling capability is sufficient as shown in Fig. 4(b).

External transistion of signal and ground connections from the chip to outside world, i.e. printed circuit board (PCB), are realized using bond pads made of top metal layer. These bond pads are then connected to PCB with the help of bond wires or solder balls. Parasitic inductance (~ 100 s of pH) and resistance associated with bond wires make them non-feasible for most of the mmWave appli- cations. Contrarily, solder balls have very low parasitic inductance (~ 10 s of pH) [12] from the connections when connected in flip chip orientation as shown in Fig. 5(a). When designing the mmWave circuit blocks (passive or active), extracted models of these signal and ground transitions should be included in the simulations. An RF ground can also be defined outside the chip, i.e. PCB, considering the IC is connected on the PCB as flipped chip using solder balls as shown in Fig. 5(b). In such case, top PCB layer (RF ground) interfacing with IC should be part of the EM simulations. This type of RF ground has minimum transition between PCB and IC and represents more realistic simulation environment towards real implementation.

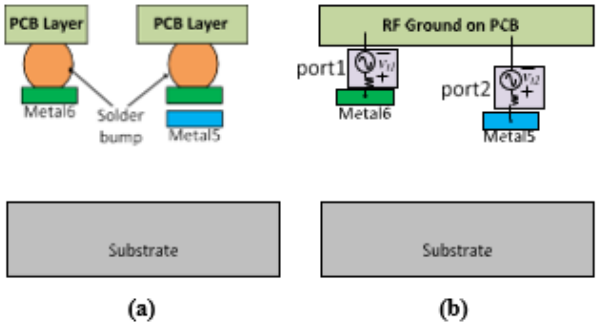


Fig. 5 Definition of ground reference in passive design

2.4 Return currents

Depending on the definition of the RF ground, an excitation current from a port finds multiple return paths as shown in Fig. 6 [13]. All these paths have finite impedance (resis- tance and inductance) and their lengths are different from each other. The final inductance and quality factor of the inductor highly depends on the impedance of these paths and their characteristics, e.g. inductance, resistance, length of the path, etc. For example, the current i_{t1} from source v_{t1} (port 1) travels towards output source v_{t2} (considering port2 is shorted to ground) through the inductor and it takes 4 different return paths to reach back to its source v_{t1}. Cur- rents i_{r1} and i_{r2} travels through ground plane by passing through voltage source v_{t2}. Ground plane is capacitively coupled with the inductor conductor, due to which electric currents (i_{r3} and i_{r4}) are induced in the ground plane. Intensity of these currents and coupling depends on the distance (d) between the inductor and ground plane. Another current i_{r5} is induced in the substrate from capacitive coupling from inductor and the substrate under the structure and it flows through the substrate and into the global ground plane through the nearest via from substrate to metal ground plane. Magnitude of this current depends on substrate characteristics, i.e. high-resistive substrate substantially reduces this current due to high resistance and reduced electric coupling compared to low-ohmic sub- strates. All these currents see different impedance when travelling through their respective medium. The effects of these return currents and their dependency on distance d can be observed from Fig. 7. An inductor is simulated with a ground plane around it for different values of d (with design an amplifier covering a broad range of frequencies, a higher-order resonator design is required which occupies large silicon area when using lumped elements. A cascaded design approach consisting of multiple narrowband stages can also be utilized to cover wideband frequency range [14]. Contrarily, transformers inherit the properties of high- order resonator design with comparatively compact layout area. A generic schematic of a transformer is shown in Fig. 8(a). It has an additional mutual inductance associated with the mutual coupling (k) between its primary (L_P) and secondary L_S windings. Transformers are frequently used for mmWave designs due to their several benefits, e.g. compact area, seamless signal routing, balancing/unbal- ancing (balun), AC coupling, impedance transformation, etc. Moreover, a transformer can also be used in narrow- band operations. A transformer-based LC resonator in Fig. 8(b) produces resonances at two different frequencies which can be calculated as the case with no ground plane. From this example, it can be deduced that a ground plane has almost no effect when its distance from coil is greater than its radius.

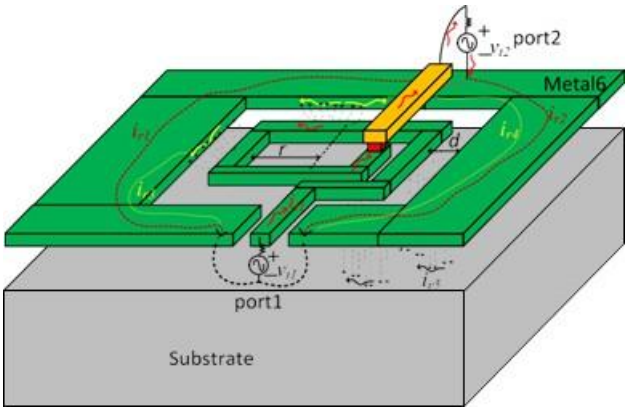


Fig. 6 Visualization of return currents of an inductor implemented with ground ring

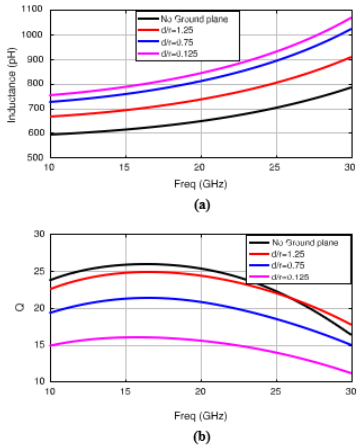


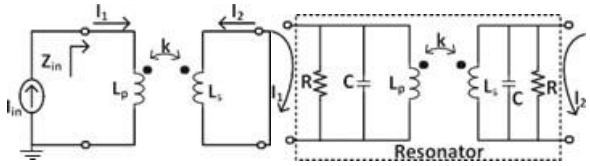
Fig. 7 a Inductance and b quality factor of an inductor with ground plane for different d/r ratios

$$\omega_L = \frac{1}{\sqrt{LC(1+|k|}}, \quad \omega_H = \frac{1}{\sqrt{LC(1-|k|}}, \quad |k| = \frac{\omega_H^2 + \omega_L^2}{\omega_H^2 - \omega_L^2}, \tag{3}$$

2.5 Applying transformers in mmWave IC designs

In narrow band amplifier designs, a parallel LC based resonator is utilized which offers cancellation of capacitive reactance of the transistor at its output ($C_{parasitic}$) which results in maximum gain from the transistor at resonance frequency of the resonator. Losses in the resonator ele- ments (quality factor), i.e. inductor (L) and capacitor (C), limit this gain. These losses increase significantly at mmWave frequencies due to associated parasitic effects,

e.g. skin effect, eddy current, capacitive coupling with neighbouring structures, etc. Quality factor of inductors (Q_L) can be improved by custom made design and optimized layout techniques. However, quality factor of capacitors (Q_C) degrades with the increase in their area. Therefore, big capacitors should be avoided in the resonators at mmWave frequency operations. In order to where x_L and x_H are lower and higher resonance frequencies, respectively. It can be observed from Eq. 3, that separation between x_L and x_H can be controlled with k. Simulated magnitude of impedance of this resonator is shown in Fig. 9 with different values of k. It can be seen that for lower k, the two resonances come closer to each other. This feature is useful for wideband amplifier designs as in [15] and [3]. However, when the k is increased sep- aration between two resonances starts to increase which is a suitable criteria for narrowband amplifier designs. In such case, only one resonance frequency (for example, x_L) is used. Different types of layout techniques are used to achieve the desired coupling, for example, interleaved layout design (horizontal coupling) and multi-layer design (for vertical coupling) [16]. The design of the transformer layout highly depends on the available metal layers and



(a) **(b)**

Fig. 8 a Transformer schematic, b transformer-based resonator

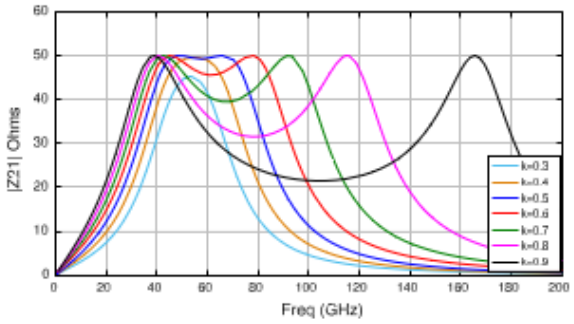


Fig. 9 Impedance of a transformer with varying coupling their respective properties (i.e. thickness, sheet resistance, etc.).

3 LNA design

In order to optimize the input noise of the LNA towards minimum noise figure (NF_{min}), two main factors are considered, i.e. optimum noise match and minimizing the intrinsic and extrinsic gate resistance. Intrinsic gate resis- tance is optimized by optimizing the number of gate fingers and by increasing the poly to M1 contacts of the gate fin- gers. Extrinsic gate resistance is reduced by optimizing the transition of gate from M1 to higher metal layers increasing the number of M1 to M5 vias. Proposed multi-gate tech- nique of cascode device layout as discussed in Sect. 2 helps to reduce the wiring resistance at the gate terminal and can be useful for low noise amplifier designs.

An inductively degenerated common source cascode LNA is designed using multigate layout technique. The proposed LNA is fabricated using 45 nm CMOS SOI technology at center frequency of 33 GHz. Schematics of the designed LNA is shown in Fig. 10. A unit cell of cascode connected devices is designed first and then a bigger device is designed based on these unit cells. In addition to the fast active devices, high quality factor passive structures play a key role in mmWave frequency designs. CMOS SOI technology provides not only benefits of reduced parasitics, higher f_{max} for active devices, but also offers high resistive substrate that allows the design of low loss passive structures. Presumably, CMOS SOI technology is being considered as an attractive choice for future mmWave integrated system designs. Moreover, availability of two thick metal layers in metal stack offers additional design freedom towards low-ohmic passive structures, such as inductors, transmission lines, trans- formers and various interconnects.

In this design, a narrowband input matching approach is used. Source inductance is realized by coplanar waveguide (CPW) transmission line, and a custom inductor is used for gate inductance. Layout of the gate inductor is similar to Fig. 6. CPW transmission line (TL) is designed using thick copper layer of M8. Since the required degeneration inductance is small, use of CPW TL provides benefits of lower inductance with compact area integration.

A one turn transformer with high k is used to resonate the capacitance at the drain of the cascode devices. Vertical coupling between the primary and secondary coils is achieved by stacking the M6 and M7 as shown in Fig. 11.

Transformer was designed for maximum coupling ($k \sim 0.84$) that produces two resonances separated far from each other and only the lower resonance at 33 GHz is used (also shown in Fig. 9, black trace). Ground reference port definition strategy discussed in Sect. 3, is used for EM simulations of the passive structures. Transformer is also performing balun function, providing differential signal at the output of the first stage. An output differential buffer with the similar transformer load is used as the second stage of the LNA.

4 Measurement results

In order to make a comparison of multi-gate cascode device with conventional style layout, two separate struc- tures are fabricated using 45 nm CMOS SOI technology. The first device is using conventional style layout, and the second device utilizes multi-gate technique. Schematic of the measurement configurations and die micrographs of both structures are shown in Fig. 12. S-parameter mea- surements are performed from 30 to 50 GHz frequency range, using Keysight 67 GHz PNA. GSG pads and probes are used to measure the s-parameters at the input and output. Two port calibration is performed up to the probe tip using external through-reflect-load (TRL) standards on a separate calibration substrate. DC biasing for gate and drain of the structures are provided using bias-T from external sources. However, biasing of cascoded transistors are provided from on-chip power supply (VDD = 1 V) with enough decoupling

capacitors. Measurement results include the input and output pads and extended transmis- sion lines up to the device terminals.

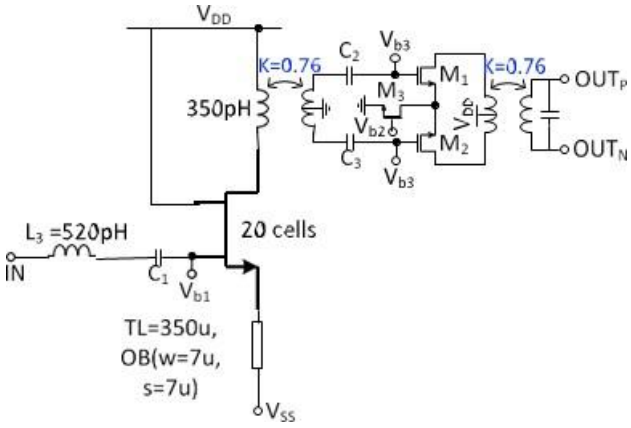


Fig. 10 Schematic of the LNA

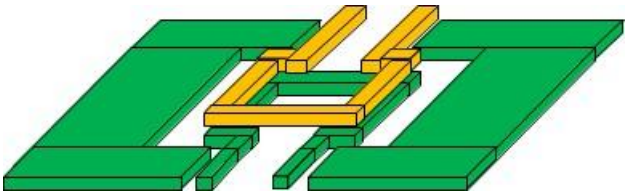


Fig. 11 3D layout view of a 1 turn transformer with lateral coupling

Gate resistance of the structures are extracted from the measured s-parameters (at fixed bias voltage of 580 mV) using real part of h_{11} as also used in [9] and plotted in Fig. 13.

$$r_g = Re(h_{11}) \quad (4)$$

Gate capacitance (C_{gs} and C_{gd}) and transconductance (g_m) are extracted using following equations [17],

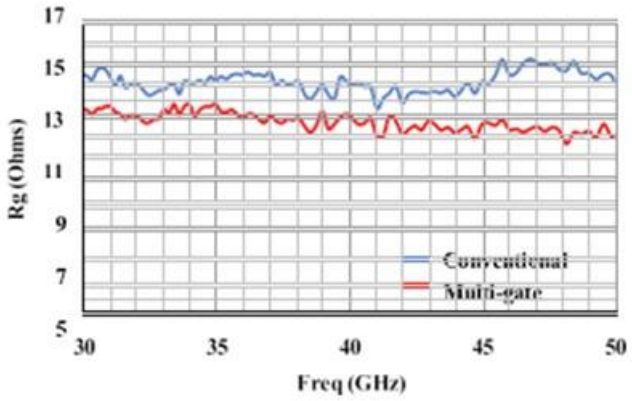


Fig. 13 Extracted R_g of two structures (VDD = 1 V, V_{bias} = 580 mV)

$$C_{gs} \; C_{\_} = \frac{Im(y_{11}+y_{12})}{} \times \frac{Im(y_{12})}{} \quad (5)$$

$$_{gd} = \text{—} \quad \text{x}$$

$$g_m = Re(y_{21})$$

Extracted gate resistance of the multi-gate layout technique is 10% lower than the conventional layout style. However, due to the increased wiring of the multi-gate technique, gate to source (C_{gs}) and gate-to-drain

capacitance (C_{gd}) are 4% and 40% higher than in the conventional layout, as shown in Fig. 14. There is roughly no change in the transconductance of both structures, as shown in Fig. 15. Due to the increase in Cgg, fmax of multi-gate device is 20% lower than the conventional layout as shown in Fig. 16. However, this is still sufficient for targeted frequency bands. Since the detailed modelling for multigate devices differs from the conventional transistors, measurements instead of simulations are used for comparison between two structures. Table 2 shows comparison results of extracted parameters at 33 GHz for the two structures (Fig. 12).

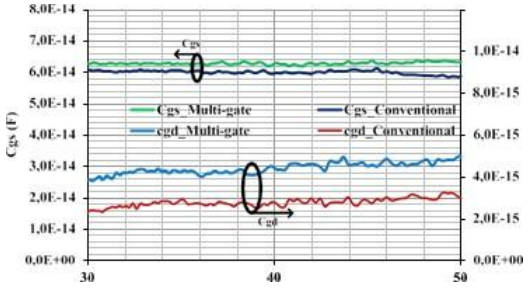


Fig. 14 Extracted capacitances, C_{gs} and C_{gd} of two structures, (VDD = 1 V, V_{bias} = 580 mV)

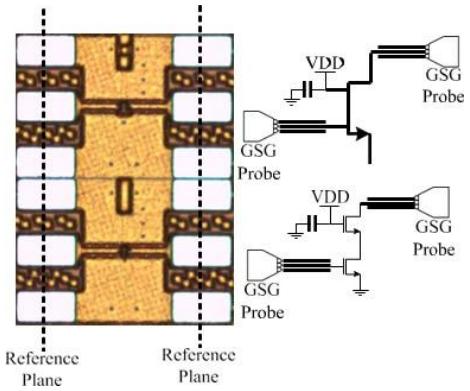


Fig. 12 Die micrographs of cascode structures and respective schematics

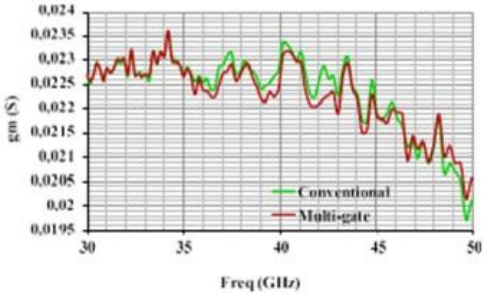


Fig. 15 Extracted g_m of two structures, (VDD = 1 V, V_{bias} = 580 mV)

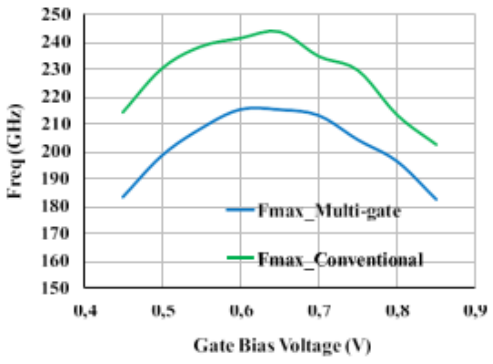


Fig. 16 Extracted f_{max} versus V_{bias} of two structures

A single-ended input, differential output LNA is fabri- cated using GlobalFoundries 45 nm CMOS SOI technol- ogy. Die micrograph of LNA is shown in Fig. 17, core area including input and output pads is $1061 \times 0.349\ \text{mm}^2$.

Although, it is better to compare the layout effects of two

styles on the noise performance of an LNA. However, this was not possible due to the limited available resources for chip fabrication. GSG probes are used to perform on wafer measurements. LNA is measured from a single-ended input to a single-ended output because of the non availability of single-to-differential probe calibration. S-parameters of the LNA are measured using Keysight 67 GHz PNA. Noise figure measurements are performed using 50 GHz noise source, 50 GHz spectrum analyzer and pre-amplifier pro- vided by Keysight technologies. Calibration of the noise figure measurement setup is performed using on-chip through standard. Biasing of the active blocks is imple- mented using local current mirrors which take 100 lm current from off-chip external source using bondwire connections. Biasing voltage is controlled using on-chip integrated shift register logic. Supply voltage is also routed from external supply using bondwire connections with sufficient supply de-coupling capacitance placed on- and off-chip. Measured and simulated s-parameters and noise figure results for dual-gate LNA are shown in Fig. 18(a, b), respectively. Measured S21 gain is 10.2 dB at 33 GHz. Measured input (S11) and output (S22) reflection coeffi- cient are below – 10 dB at 33 GHz. Noise figure is 4.3 dB at 33 GHz. Table 3 shows a brief performance comparison of the LNA with existing state-of-the-art (SOA) designs at 33 GHz. Measured (and simulated) gain of the LNA is around 3 dB lower because it was measured (and simu- lated) from single-ended output only. It shows that LNA is having much lower power consumption with the LNA's of similar performance.

Table 2 Comparison table of extracted parameter values at 33 GHz (VDD = 1 V, V_{bias} = 580 mV)

Parameters	Conventional	Multigate
R_g (X)	14.3	12.9
C_{gs} (fF)	60	62
C_{gd} (fF)	2.77	4.33
g_m (mS)	22.5	22.5
f_{max} (GHz)	243	215

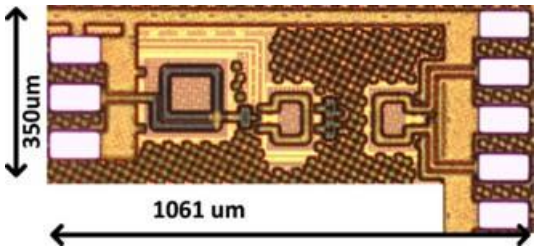
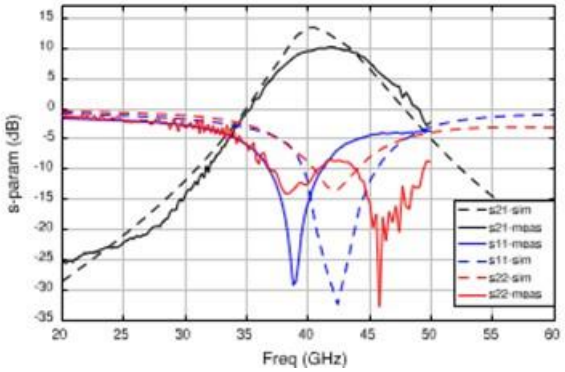
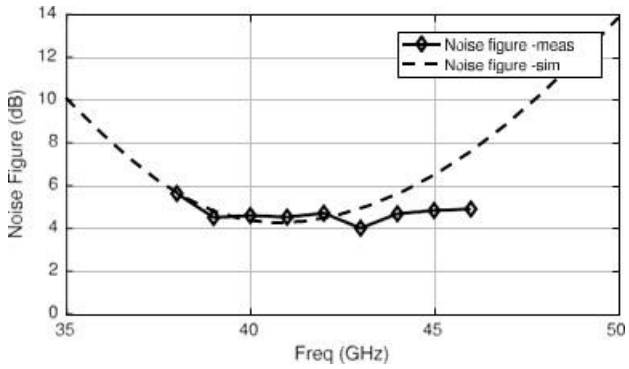


Fig. 17 Micrograph of the LNA



(a)



(b)

Fig. 18 Measured s-parameters of LNA

Table 3 Perfomrance comparison of LNA with existing SOA LNAs

Technology	This work 45 nm SOI	[18] 130 nm CMOS	[19] 90 nm CMOS	[20] 65 nm CMOS	[21] 90 nm SOI
Freq (GHz)	28	30	32	33	28–33
Max. gain (dB)	10.2	12.6	13.8	14.3	11.9
NF (dB)	4.2	4	3.8	6	4.2
P_{diss} (mW)	13	24	18	43.2	40.8
P_{1dB} (dBm)	-11	N/A	N/A	N/A	N/A
Chip area (mm^2)	0.31	0.252	0.48	0.286	0.18

5 Conclusion

This work introduces layout optimization techniques of cascode connected transistors and a design of an LNA for mmWave applications. A multi-gate layout technique is compared to a conventional layout style. Optimization of intrinsic and extrinsic parasitic components for both cas- code devices is discussed. Design techniques of silicon based passive structures for mmWave applications are discussed and optimization of ground connection pre- sented. An overview was given for setting up the ground reference for port definition in EM simulation tools. Design of a 33 GHz LNA using multi-gate cascode device is also presented including key results from fabricated sample. A multi-gate layout reduces gate resistance while conven- tional layout reduces wiring capacitance. It is compared against cascode LNA's. The device is designed and fabri- cated using 45 nm CMOS SOI technology. Measurement results show a reduction of 10% in gate resistance of multi- gate layout technique compared to the conventional double contacted gate approach. However, gate-to-source and gate-to-drain capacitances are degraded by 4% and 36%, respectively, which limits the maximum speed of the input stage. Therefore, this comparison concludes that there is a trade-off in optimization between r_g and f_{max} of the cascode devices in layout designs. Measured results of LNA achieve a peak gain of 10.2 dB and noise figure of 4.2 dB at 33 GHz.

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