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A Novel Ultra Low Power and Highly Stable SRAM Bit-Cell for High-Speed Applications Using 45nm Technology Node

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Abstract - Modern system-on-chip applications demand SRAMs that not only operate at high speeds and offer robust stability but also prioritize energy efficiency for prolonged functionality. In this research, various SRAM cell architectures are explored, with particular emphasis on a newly proposed 9T SRAM bit-cell. Key parameters analyzed include leakage power, read and write delays, and static noise margins (WSNM and RSNM). Simulation outcomes indicate that the proposed 9T SRAM cell achieves the highest RSNM among all layouts, while the 8T SRAM cell records superior WSNM, attributed to its use of p-type access transistors. Furthermore, the 8T cell delivers reduced write delays when compared to the other designs. Notably, the 9T SRAM cell also demonstrates the lowest leakage power across all examined topologies. The fabrication of these SRAM bit cells was carried out using gpdk 45nm technology in the Cadence Virtuoso environment.

Keywords - *SRAM Cell, Static Noise Margin, Read Delay, Write Delay, Leakage power.*

I. INTRODUCTION

Static Random-Access Memory (SRAM) plays a vital role in System-on-Chip (SoC) architectures because of its flexibility in logic integration and prevalent use within contemporary high-performance applications [1]. As technology continues to scale, there have been notable enhancements in device capabilities, power efficiency, and chip area due to the miniaturization of device features. Yet, this reduction in process node sizes introduces new challenges, including increased susceptibility to circuit disturbances and reliability concerns [2]. In response, recent studies have increasingly emphasized the design of memory circuits that are optimized for low power operation—addressing the energy constraints typical of battery-powered electronics. For such devices, memory modules are required to balance strict energy efficiency and dependability standards as they process large amounts of data and strive for extended battery lifetime. The use of complementary metal oxide semiconductor (CMOS) processes further supports greater integration density and faster operational speeds. However, these advancements come hand-in-hand with issues like enhanced leakage currents and reduced robustness. A proven strategy for combating leakage is to lower the supply voltage, which directly minimizes overall power usage and substantially cuts down leakage current levels [3].

The 6T SRAM cell is widely adopted in circuit designs due to its compact, symmetrical structure and rapid differential sensing capabilities. However, conventional 6T cells operating in the subthreshold regime encounter challenges in write, read, and retention modes, largely due to significant threshold voltage (Vt) fluctuations arising from process, voltage, and temperature (PVT) variations in advanced ultrashort-channel technologies [4]. Such cells display heightened vulnerability to PVT shifts, given the exponential dependence of subthreshold current on both gate-to-source voltage (VGS) and threshold voltage (Vt) [5]-[8].

Conventional SRAM cells often face instability issues during both data writing and reading operations [9]. As device scaling progresses into smaller CMOS technology nodes, numerous challenges arise with the standard 6T SRAM cell design, including increased variability, compromised read stability, and elevated hold

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power and leakage currents [10]. Among the various influencing factors, supply voltage and transistor sizing remain crucial parameters [11]. Although lowering the supply voltage is a prevalent technique to reduce power consumption, it typically requires a corresponding decrease in threshold voltage to maintain performance. This reduction, however, leads to an exponential rise in subthreshold leakage current, thus increasing static power dissipation. Due to their favourable balance of speed and low power usage, SRAM-based caches are widely adopted in system-on-chip designs, especially for portable electronics. Given that cache memories can occupy over half of a microprocessor's silicon area, leakage power from the cache significantly impacts the processor's total power consumption [12].

Operating SRAM bit cells at reduced supply voltages (VDD) often results in a decline in static noise margin (SNM) and a concurrent reduction in cell speed [13]. This study presents a comparative analysis of multiple SRAM architectures—including 6-transistor (6T), 8-transistor (8T), 10-transistor (10T and 10T-Dohar), 12-transistor (12T), as well as the proposed 9-transistor (P9T) SRAM cells—evaluated against key performance metrics such as leakage power, high static noise margin (HSNM), read static noise margin (RSNM), write static noise margin (WSNM), read delay, and write delay.

II. CIRCUIT DESIGN AND ANALYSIS

A. Six Transistor (6T) SRAM Cell Design

In a conventional 6T SRAM cell, data at Node Q and Node QB retain its value as access transistors (N3 and N4) are off during hold mode [14].

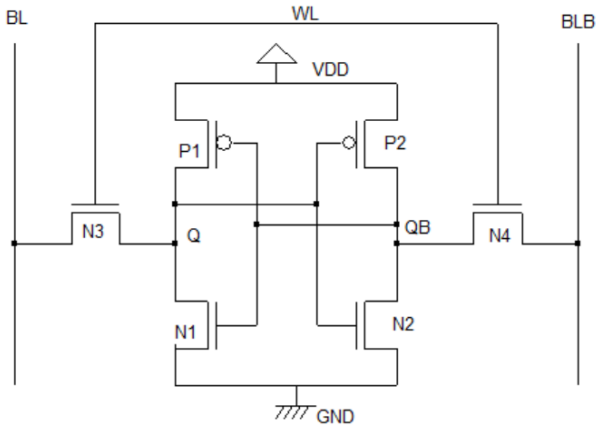


Fig. 1 6T SRAM cell [14]

In the write operation of an SRAM cell, it is essential that the ratio of the pass-gate transistor strength to the pull-up transistor strength—known as the cell gamma ratio is sufficiently large. Initially, the bit-lines (BL and BLB) are driven to complementary voltages, after which the wordline (WL) is asserted. The input data is then applied to the BL line. When the access transistors (N3 and N4) are turned on by the activated WL, the data present on the bit-line is successfully written into the memory cell.

During the read operation, a crucial requirement is that the pull-down transistor's drive current must be considerably stronger than that of the pass-gate transistor; this is referred to as the cell beta ratio. Typically, both bit-lines (BL and BLB) are precharged to a high voltage level, usually VDD. The wordline is then driven high, enabling the read process where the stored data influences the state of BL and BLB. The resulting differential signal on the bit-lines is detected by a sense amplifier, which produces the corresponding output.

B. Eight Transistor (8T) SRAM Cell Design [15]

Compared to conventional 6T SRAM cells, the fully differential 8-transistor (8T) SRAM cell is employed to enhance read stability, improve write capability, and achieve faster data transfer speeds without increasing leakage power. As shown in Figure 2, the 8T SRAM cell builds upon the core 6T SRAM structure by adding two additional p-type transistors, P3 and P4, which are connected in parallel with the existing n-type access transistors that interface with the bitlines. During write operations, the n-type bitline access transistors are

controlled by the wordline (WL) signal, while the p-type bitline access transistors are governed by the read wordline (RWL) signal. In the memory array, a single word line (WL) selects individual cells, whereas the read wordline (RWL) controls groups of cells.

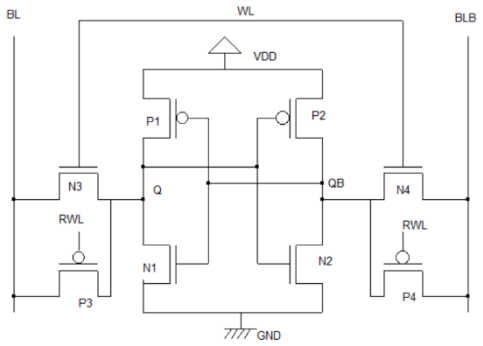


Fig. 2 8T SRAM cell [15]

The read operation of the 8T SRAM cell, much like that of a conventional 6T SRAM cell, utilizes a differential sensing approach. When the cell is idle, the read wordline (RWL) is held at VDD, and the wordline (WL) is maintained at VGND. Before initiating a read, the bitlines are precharged to VDD. The read process starts when the RWL transitions from VDD to VGND, turning on the read bitline access transistors (P3 and P4). If node Q stores a logic '0', the transistor path through P3 and N1 causes the bitline (BL) to discharge. A sense amplifier connected to BL and its complement BLB detects the stored data by sensing the voltage difference. Due to lower hole mobility, the p-type bitline access transistors (P3 and P4) inherently have less drive strength compared to the pull-down transistors (N1 and N2). Additionally, the p-type access transistor corresponding to a stored '1' helps strengthen the pull-up action during reads.

For the write operation in the 8T SRAM cell, the incoming data and its complement are first transferred to the bitlines, with one bitline driven down to 0 V. The write is triggered by setting WL to VDD and RWL to VGND. Data is then written into the cell through the write bitline transmission gates. This configuration of the 8T SRAM cell enhances the voltage margin and accelerates data writing when compared to the traditional 6T SRAM design.

C. *Ten Transistor (10T) SRAM Cell Design* [16]

The write and hold operations of the 10T SRAM bit-cell are quite similar to those in the traditional 6T SRAM cell because the 10T configuration maintains a nearly identical circuit topology during these modes. Notably, during both hold and write phases, the ground voltage (VGND) is held at the supply voltage level (VDD), a measure taken to minimize leakage current through the bitlines.

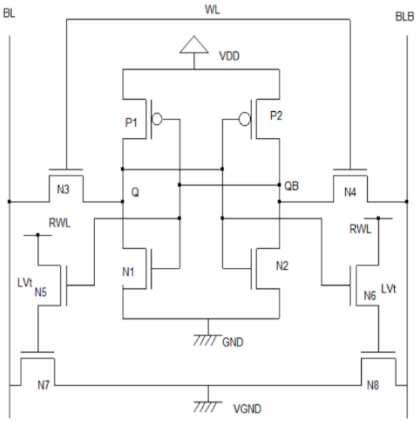


Fig.3 10T SRAM cell [16]

During the read process, activating the read wordline (RWL) pulls VGND down to ground, enabling the bitline to discharge. Since the data node Q is separated from the bitline BL by transistors N5 and N7, the read current bypasses the storage node Q and instead passes through transistor N7. As a result, the static noise margin (SNM) of the bit cell remains largely unaffected between read and hold operations. Furthermore, the bitline discharge path involves only a single access transistor (N7), and the use of low-threshold voltage (low VT) transistors for N5 and N6 contributes to a reduction in read delay.

D. *Ten Transistor (10T-Dohar) SRAM Cell Design* [17]

During the hold operation, the wordline (WL) is deactivated, causing the access transistors (N5 and N6) to switch off. This allows the cell core to retain the stored data at nodes Q and QB without disturbance.

In the read operation, the precharge circuit drives both bit-lines (BL and BLB) to a high voltage level (VDD). Subsequently, the WL is asserted, turning on the access transistors (N5 and N6). If node Q holds a logic low, bit-line BL discharges through transistors N5 and N1, while BLB remains at its precharged level. It is crucial to note that nodes S and S' remain stable and unaffected throughout the read cycle. The data on BL and BLB is then conveyed to a differential sense amplifier for detection. For reliable read performance, the width-to-length (W/L) ratio of the access transistors should be smaller than that of the pull-down transistors to maintain proper signal integrity.

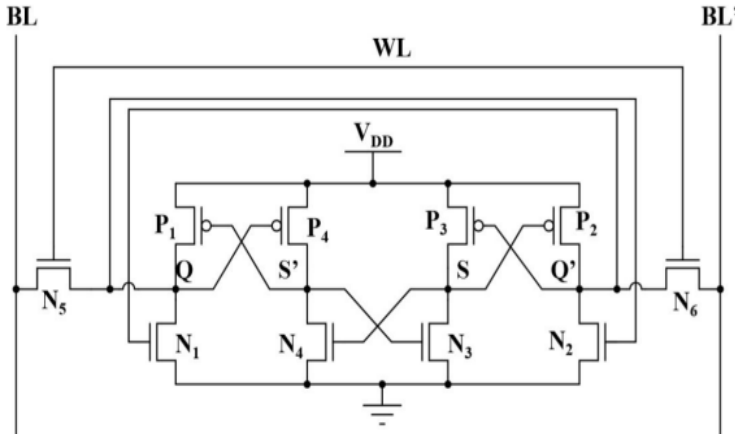


Fig. 4 10T-Dohar SRAM cell [17]

During the write ‘0’ operation, assume that nodes Q, Q', S, and S' initially hold the values ‘1’, ‘0’, ‘1’, and ‘0’, respectively. To write a ‘0’ at node Q, the bit-lines are set such that BL = ‘0’ and BLB = ‘1’. The voltage at node Q is driven low to ‘0’ via BL through the access transistor N5, while node QB is driven high to ‘1’ via BLB through access transistor N6. As the write cycle concludes, the data stored at nodes Q, Q', S, and S' updates to ‘0’, ‘1’, ‘0’, and ‘1’, respectively. For the write operation to be effective, the width-to-length (W/L) ratio of the access transistors must exceed that of the pull-up transistors.

E. *Twelve Transistor (12T) SRAM Cell Design* [18]

In the 12T SRAM cell, assume that the initial logic states of nodes Q, QB, S, and SB are ‘0’, ‘1’, ‘0’, and ‘1’, respectively. During the hold operation, the word line (WL) is deactivated, turning off the access transistors (N5 through N8). This ensures that the cell core retains the stored data at nodes Q and QB without disturbance.

For the read operation, the precharge circuit sets both bit-lines (BL and BLB) to a high logic level. The WL is then asserted, activating the access transistors (N5–N8). If node Q holds a low logic value (‘0’), the bit-line BL discharges through transistors N5 and N1, while BLB remains at its precharged high level. This voltage

difference between BL and BLB is then detected by the differential sense amplifier, allowing the stored data ‘0’ to be read correctly. It is important to note that the states of nodes S and SB remain stable and unchanged throughout the read process.

During the write operation, the wordline (WL) is asserted. Suppose the cell initially stores a logic ‘0’, which corresponds to nodes Q, QB, S, and SB holding ‘1’, ‘0’, ‘1’, and ‘0’, respectively. To write a ‘0’ at node Q, the bitlines are set such that BL = ‘0’ and BLB = ‘1’. As a result, node Q is driven low to ‘0’ through transistor N5 by BL, while node QB is driven high to ‘1’ by BLB through transistor N6. At the same time, node S discharges to ‘0’ via transistor N7, and node SB charges to ‘1’ via transistor N8, completing the write process for those storage nodes.

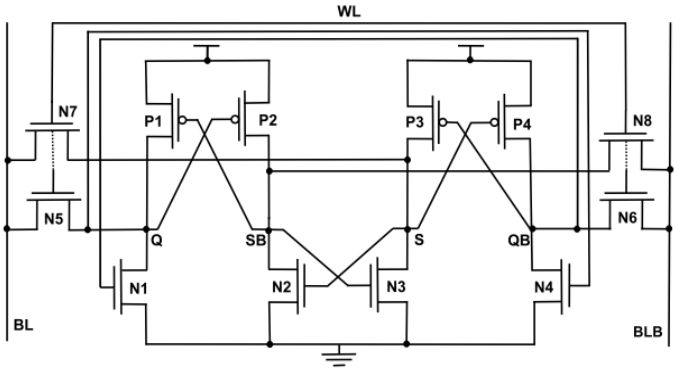


Fig. 5 12T SRAM cell [18]

This process facilitates an efficient writing operation. It is crucial to note that the access transistors play a more critical role than the pull-up transistors in ensuring a satisfactory write operation.

F. *Proposed 9T SRAM Cell Design and its operation*

Control Signal	Hold Mode	Read Mode	Write Mode ‘0’/’1’ @ Q
WL	GND	GND	VDD
RWL	VDD	GND	VDD
BL	VDD	VDD	GND/VDD
BLB	VDD	VDD	VDD/GND
RBL	VDD	Precharged	VDD

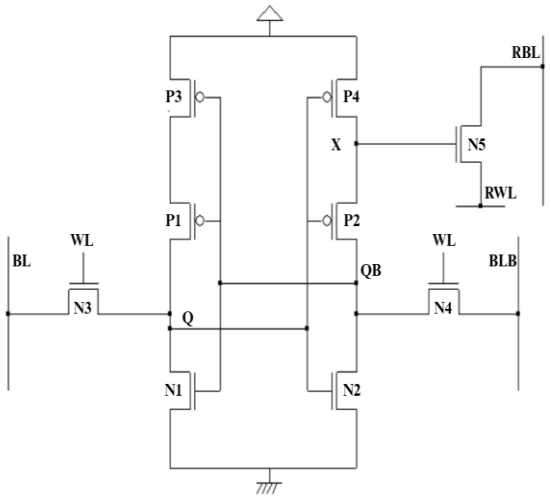


Fig. 6 Proposed 9T SRAM bit-cell and status of control signal

In the proposed 9-transistor (9T) SRAM cell, during the hold state, the wordline (WL) is held at a low logic level (GND), while the read wordline

(RWL) is maintained at a high logic level (VDD). This control scheme effectively disconnects the excess access transistors N3 and N4 from the SRAM core, isolating the storage nodes from the read bitline (RBL). Since RWL is at VDD, the read bitline remains charged and does not discharge unintentionally, eliminating any unnecessary power loss through leakage currents on the read path. Furthermore, within the cell core, a PPN transistor stack architecture is implemented, which is well-known for its leakage reduction properties due to the stacking effect that suppresses subthreshold leakage currents. Together, these factors contribute to significant suppression of leakage power during standby or hold mode, making the P9T cell exceptionally energy-efficient while reliably retaining the stored data at nodes Q and QB.

Before commencing a read operation, the read bitline (RBL) is precharged to the supply voltage (VDD) to establish a known initial condition. At this point, assume the SRAM cell stores complementary data, specifically logic '0' at node Q and logic '1' at node QB. Due to the stored '0' in node Q, node X attains a corresponding high logic level, which is sufficient to switch ON transistor N5. During reading, RWL is pulled low (to GND), which enables the discharge path for the read bitline through transistor N5 exclusively. Importantly, the WL remains at GND, ensuring that nodes Q and QB stay electrically isolated from the main bitlines BL and BLB, thereby avoiding read disturb problems that often degrade stability in other SRAM architectures. This unique isolation contributes to a substantially improved read static noise margin (RSNM), which in this design is maintained at a level comparable to the static noise margin during hold operations, thereby enhancing reliability. Moreover, having only one transistor control the entire read discharge path minimizes the total read delay, allowing faster access times compared to other SRAM topologies which tend to have multiple series transistors in the read path.

In the write cycle, both WL and RWL signals are driven high to VDD, fully enabling the cell to accept new data. The write operation uses differential signaling; for example, if the objective is to write a logic '1' at node Q, the bitline BL is set to VDD and the complementary bitline BLB is set to GND. The P9T cell utilizes two series-connected PMOS transistors as pull-up devices within the storage node circuitry, a strategic design choice which helps to decrease the write delay by providing stronger pull-up drive capability. This enhanced pull-up network counters the difficulty typically encountered in overwriting the cell state, especially at low supply voltages, thereby enabling rapid and robust data writing. The overall architecture balances strong writability with low leakage and high read stability, resulting in a high-performance SRAM bit cell optimized for low power and high-speed operation in scaled 45nm CMOS processes.

III. RESULTS AND DISCUSSION

We conducted an analysis of the performance parameters of 6T, 8T, 10T, 10T-Dohar,12T SRAM cells with proposed 9T SRAM cell. All simulations were performed using industry-standard 45nm CMOS technology. We assumed a supply voltage of 1.1V and an operating temperature of 27°C unless otherwise specified. Table 1 presents the various performance parameters for all the considered SRAM cells.

A. Stability analysis

We compare the characteristics of all proposed cells in terms of writability, read stability concerning SNM, and write accessing stability. For the simulation of all SRAM cells, we chose transistor sizes of 120nm for pull-up transistors, 1500nm for pull-down transistors, and 240nm for access transistors.

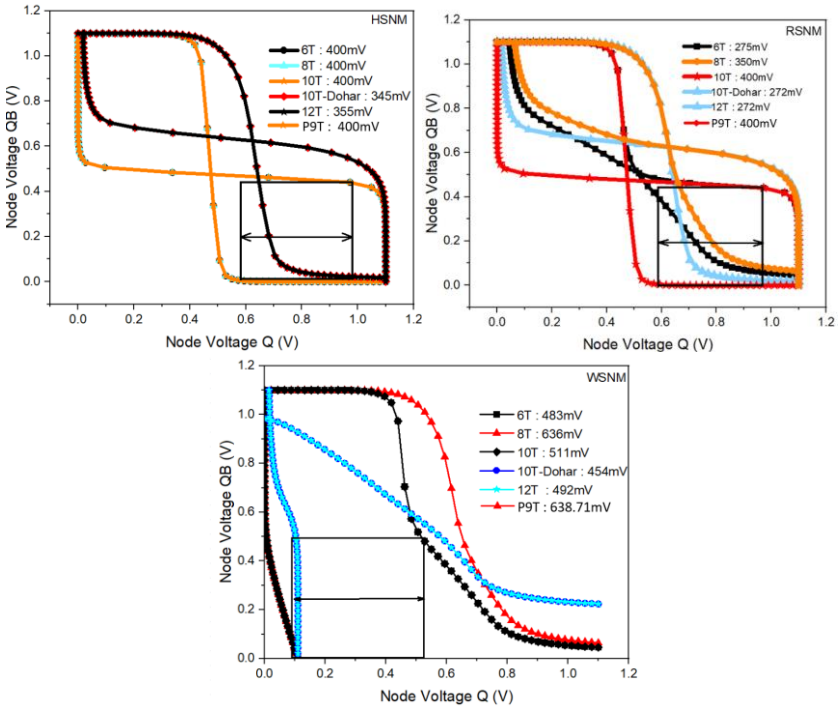
Table 1 Performance comparison of various SRAM cells based on simulations in 45-nm CMOS Technology

SRAM Cell	HSNM (mV)	RSNM (mV)	WSNM (mV)	Read delay, t_{rd} (fs)	Write delay, t_{wd} (ps)	Static power (pW)	Area (μm^2)	SEQM (values in 10 million)
6T	400.00	275.00	483.33	97.21	13.63	49.06	4.19	1037.82

8T	400.00	350.00	636.36	647.3	11.68	53.98	5.48	354.01
10T	400.00	400.00	511.00	191.87	14.32	49.09	7.31	677.9
10T-Dohar	345.45	272.72	454.54	96.59	15.15	90.51	7.90	175.25
12T	355.55	272.72	492.3	97.08	13.63	98.13	8.24	212.98
P9T	400.00	400.00	637.71	32.91	12.67	24.04	6.75	

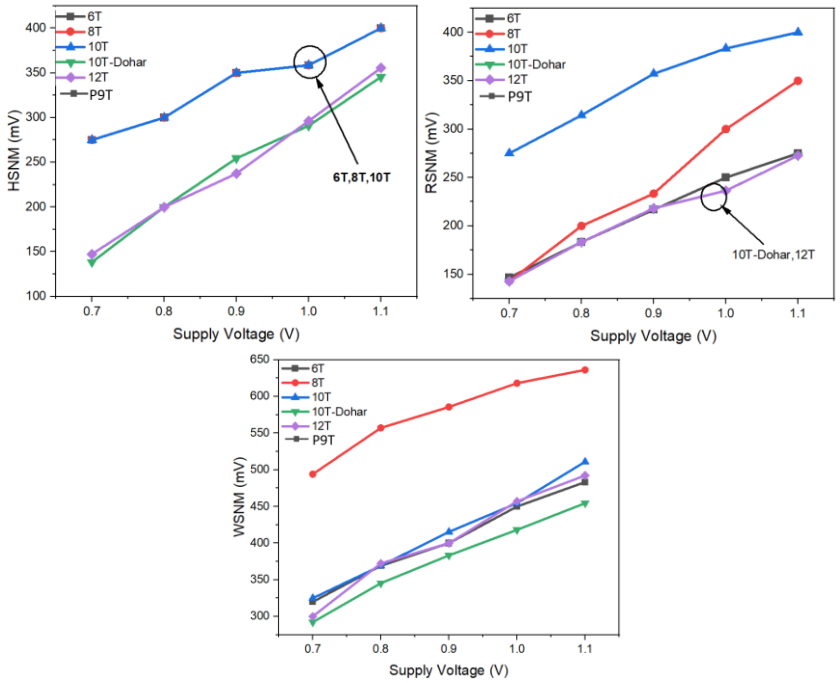
To improve writing capability, the pull-down transistors are strengthened. This enhancement involves adjusting the pull-up ratio (PR), which represents the ratio between pull-up transistors and access transistors, and the bit cell ratio (CR), representing the ratio between pull-down transistors and access transistors. Specifically, PR is set to 0.5, while CR is set to 6.25. These adjustments aim to enhance stability in the system.

From the results, we observe that the 6T, 8T,10T and P9T SRAM cells provide better hold stability (HSNM) compared to the 10T-Dohar and 12T SRAM cells. The read static noise margin (RSNM) of the 10T SRAM cell is higher than all other considered SRAM cells due to its isolated node. The write static noise margin (WSNM) of the 8T SRAM cell is higher than other SRAM cells because both n-type and p-type data access transistors are turned ON during write operations, improving stability. However, the WSNM of the 12T SRAM is marginally higher than that of the 10T-Dohar due to additional access transistors (N7, N8). For a fair comparison, we evaluated the HSNM, RSNM, and WSNM of all the considered SRAM cells at different supply voltages, as shown in Fig. 7.



(a) (b) (c)

Fig. 7 (a) HSNM (b) RSNM (c) WSNM



(a) (b) (c)

Fig. 8 Effect of supply voltage variation on (a) HSNM (b) RSNM (c) WSNM

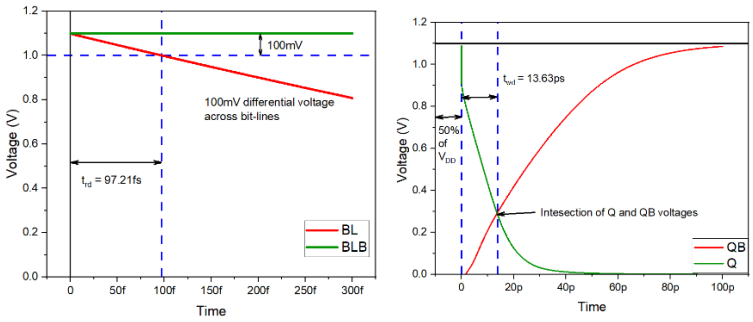
B. *Delay analysis*

The read access time, also referred to as read delay (trd), represents the time interval during which the bit-lines BL and BLB show a voltage difference of 100 mV, as depicted in Fig. 8(a) [19].

Table 1 compares different SRAM bit-cell architectures and reveals that the 8T SRAM cell experiences a longer read delay, primarily due to the inclusion of p-type access transistors (P3 and P4). Since read current (Iread) directly influences read delay performance, the lower hole mobility in these p-type transistors results in a reduced Iread for the 8T cell, thereby increasing its read delay. Conversely, the 6T, 10T-Dohar, and 12T SRAM cells exhibit similar read delays because they share an identical Iread conduction path. The proposed 9T (P9T) SRAM cell achieves the shortest read delay owing to its read current path consisting of only a single transistor.

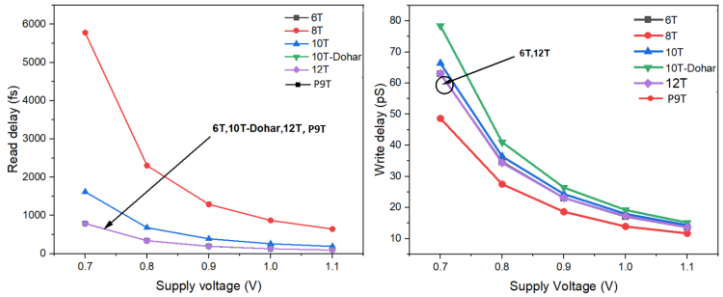
Similar to the read access time, the write access time, also known as write delay (twd), is defined as the time interval between the intersection of two storage nodes (Q and QB) and the moment the supply voltage (WL) reaches 50%, as shown in Fig. 8(b).[19].

The 8T SRAM bit-cell exhibits reduced delay compared to other bit-cell designs because incoming data is efficiently transferred through transmission gates consisting of both n-type and p-type access transistors. On the other hand, the 10T SRAM bit-cell experiences a slightly higher delay than the 6T design, primarily due to the increased capacitance at its storage nodes. For the 6T and 12T SRAM cells, the write delay remains nearly the same since both utilize an identical write path. Although the 12T SRAM cell includes extra access transistors (N7 and N8), its write delay is still shorter than that of the 10T-Dohar cell. The proposed 9T (P9T) cell ranks second in write delay performance, attributed to its series-connected PMOS transistors enhancing write speed. Figure 9 illustrates the read and write delay characteristics of all the SRAM bit-cells considered, analysed across different supply voltage levels.



(a) (b)

Fig. 9 (a) Read delay (b) Write delay calculation of 6T



(a) (b)

Fig. 10 Effect of supply voltage variation on (a) Read delay (b) Write delay

C. Static power analysis

In the power budget analysis, the static power consumption for all the SRAM cells has been calculated, with the results summarized in Table 1. This static power primarily arises from leakage currents flowing through transistors that are switched off, as well as through the bit lines, while the different SRAM bit-cells remain in their hold state [20].

The results indicate that the static power dissipation of the 8T SRAM bit-cell is slightly higher than that of the 6T cell. This increase is mainly due to an additional leakage current path from the bit-line to ground (VGND) caused by the inclusion of p-type access transistors (P3 and P4). In contrast, the 10T SRAM cell experiences reduced static power during hold mode because the leakage path to the virtual ground (VGND) occurs exclusively through the access transistors N7 and N8. Nevertheless, the 10T-Dohar and 12T SRAM cells exhibit higher static power dissipation, attributed to the greater number of off-state transistors and larger potential differences within their structures. The proposed 9T (P9T) SRAM cell achieves notably low static power dissipation, benefiting from the stacked transistor arrangement in its core. Moreover, power is reduced due to considering logic high of signal RWL during hold mode. Figure 10 presents the evaluation of static power dissipation for all analysed SRAM cells across different supply voltage levels.

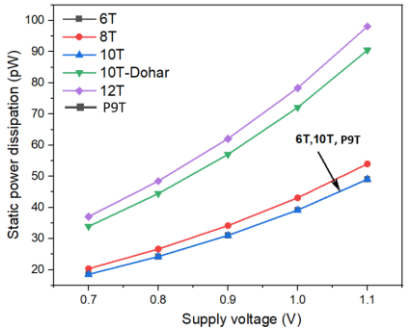


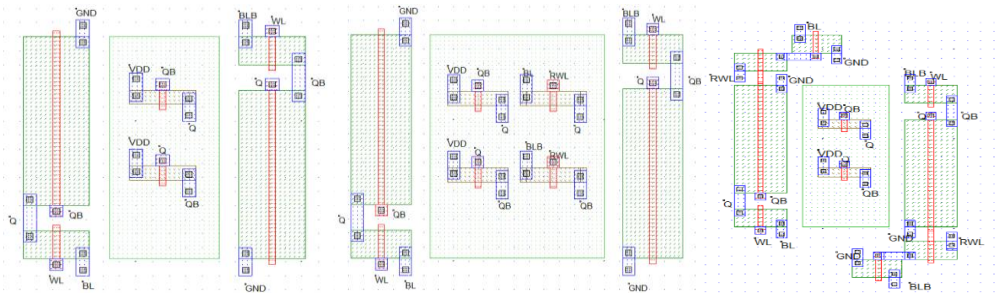
Fig. 11 Effect of supply voltage variation on static power dissipation

D. Area and Figure of merit (FOM) analysis

The silicon area occupied by MOSFET-based SRAM bit-cells is largely influenced by the total transistor count within each design. Illustrated in Figures 11 and 12 are layouts of various bit-cell configurations, crafted following MOSFET design rules. In these layouts, the minimum feature size, denoted as λ, is half the gate length. Among the designs examined, the 6T SRAM bit-cell offers the most compact footprint due to its minimal transistor count. However, the integration of an extra word line referred to as the read word line (RWL) leads to increased area requirements in other cell architectures.

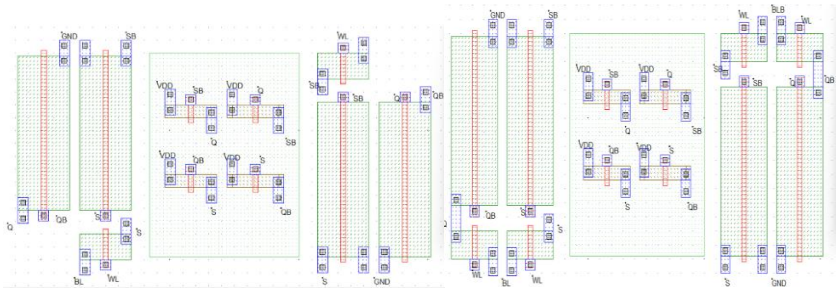
Table 1 summarizes the key performance metrics of all evaluated SRAM cells. Given the inherent trade-offs among critical performance parameters such as stability, speed, power, and area, a holistic evaluation metric known as the electrical quality metric (SEQM) was computed. This SEQM comprehensively captures the combined effects of stability, access time, physical area, and leakage power consumption. For an SRAM cell design to be considered optimal, achieving a higher SEQM value is preferred, as it indicates a better overall balance of these competing factors. The SEQM is expressed as:

$$SEQM = \frac{HSNM^2 \; X \; RSNM^2 \; X \; WSNM^2}{t_{rd} \; X \; t_{wd} \; X \; SP \; X \; Area} \quad \ldots\ldots (1)$$

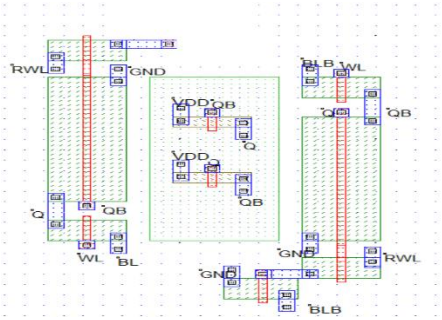


(a) (b) (c)

Fig. 12 Layout of (a) 6T (b) 8T (c) 10T SRAM cell



(a) (b)



(c)

Fig. 13 Layout of (a) 10T-Dohar (b) 12T (c) P9T SRAM cell

IV. CONCLUSION

This research systematically evaluates the performance of the conventional 6T SRAM cell alongside several advanced architectures, including the 8T, 10T, 10T-Dohar, 12T, and the newly proposed 9T (P9T) SRAM cell. The comparative analysis focuses on critical metrics such as power dissipation, read delay, write delay, write static noise margin (WSNM), and read static noise margin (RSNM). All simulations and evaluations were conducted using the Cadence simulation environment to ensure accuracy and consistency.

Among the studied topologies, the proposed 9T SRAM cell demonstrates a notably superior stability profile, exhibiting the highest RSNM. This improvement is primarily attributed to the effective isolation of the storage node from the bit line during read operations, mitigating disturbances that typically degrade stability. Additionally, the P9T cell achieves an enhanced WSNM, which can be ascribed to its innovative use of two series-connected PMOS transistors in the pull-up network, reinforcing its ability to reliably write data into the cell. In terms of speed performance, the 8T SRAM cell delivers the lowest write delay, benefiting from its efficient data access transistor configuration that accelerates the write process. However, for read operations, the P9T cell outperforms the others by achieving the shortest read delay. This advantage stems from its streamlined read path that incorporates only a single transistor, thereby minimizing the read latency and improving access times. Furthermore, when evaluating power efficiency, the proposed 9T cell stands out with the lowest leakage power dissipation among all the considered designs. This reduction is largely enabled by the stacked transistor structure within the cell core, which effectively suppresses leakage currents during idle states, making the P9T highly suitable for low-power applications.

Overall, the proposed 9T SRAM bit cell strikes an exceptional balance among power consumption, operational speed, and stability metrics, positioning it as a highly promising candidate for integration in advanced low-power, high-performance system-on-chip designs utilizing 45nm CMOS technology.

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