International Journal of
Intelligent Systems and Applications in Engineering

ISSN:2147-6799 www.ijisae.org Original Research Paper

1.

Optimization of CMOS Miller OTA using Differential Evolutionary Algorithm

Pankaj P. Prajapati*[1], Krunal P. Acharya[2], Mihir V. Shah [3]

Submitted: 19/10/2018 Accepted : 08/03/2019 Published: 20/03/2019

Abstract: The circuit parameters of CMOS based analog and mixed-signal circuits conventionally are achieved by skilled engineers. Due to the progress of Moore's assumption and the growing complication of physical MOSFET models, the attention towards automation of CMOS based analog circuit design is increased. The issue of the automatic design of analog circuit has been tracked in the academy and industry since more than last two decades. In this paper, application of differential evolution (DE) algorithm is presented for the optimization of CMOS Miller Operational Transconductance Amplifier (OTA). DE algorithm has been developed using C language to optimize the CMOS Miller OTA. The error function of optimization for this circuit depends on desired specifications like voltage gain, phase margin (PM), unit gain bandwidth (UGB), power consumption, common mode rejection ratio (CMRR), slew rate (SR), power supply rejection ratio (PSRR), and a total MOS transistor area. Ngspice circuit simulator has been used as an error function creator and evaluator. BSIM3v3 MOSFET models with 0.18 µm and 0.35 µm CMOS technology have been used to simulate this circuit. The simulation results of this work are presented and compared with previous works reported in the literature.

Keywords: *Circuit simulator, CMRR, DE algorithm, Fitness function, Optimization, PSSR, SR, UGB.*

2. Introduction

Design of a CMOS based analog and mixed-signal system is a famous topic of growing technical and economic significance [1]. There are many optimization methods presented earlier and in current time for automatic synthesis of analog circuits. A lot of research work has been devoted to evolutionary algorithm based optimization of fundamental CMOS based analog circuits such as differential amplifier, operational amplifier (op-amp), and operational transconductance amplifier (OTA). These circuits are used as the main heart of many interface circuits, like analog to digital converters (ADC), digital to analog converters, filters, and comparators. So an optimum design of fundamental CMOS based analog circuits is the basis of a design background for various applications. The main evolutionary algorithms (EA) are particle swarm optimization (PSO) [2], genetic algorithm (GA) [3], differential evolution (DE) [4], harmony search (HS) [5], ant colony optimization (ACO) [6], and artificial bee colony optimization (ABC) [7] become common in engineering applications and other fields. These algorithms have also been used to a lesser degree for optimization of CMOS based analog circuits. Some notable works are [8] [9] [10] [11]. In [8] ABC, DE and PSO algorithms were used to optimize CMOS Miller OTA. The authors concluded that DE achieves good performance than PSO, whereas ABC does not touch the goals. In [9] ABC, DE, HS, and PSO algorithms were used to optimize n^{th} order filters. The authors concluded that HS is the fastest procedures but has the maximum fault while the other procedures converged superior. In [10], the performance of HS and DE algorithms were compared, the authors also derived the same conclusion. In [11], ultra-low power CMOS Miller OTA and a three-stage CMOS Miller op-amp were optimized by GA, PSO, and a modified PSO entitled HPSO and concluded that HPSO converges better than the others. In [1], HS, standard PSO (SPSO) 1995, and SPSO 2007 were compared. The authors concluded that SPSO95 and HS deliver fast solutions getting preferred target values. DE algorithm has been used to optimize various analog circuits like CMOS voltage divider, CMOS common source amplifier, CMOS three stage current starved voltage controlled oscillator and CMOS differential amplifier with current mirror load using 0.18 µm CMOS technology [12]. PSO based methodology has been tested to size rail to rail CMOS Miller OTA using 0.35 µm and 0.18 µm standard CMOS technology parameters [13]. The performance of the modified PSO algorithm with standard PSO and ABC algorithms had been presented in [14] by optimizing bulk driven OTA and two-stage CMOS op-amp using 130 nm CMOS technology. Two-stage CMOS op-amp was designed using 0.18 µm and 0.35 µm CMOS process technology in [15].

Op-amp works well for low-frequency applications, such as audio and video systems. For higher frequencies, OTAs are used as the building blocks for analog and mixed-signal circuits such as regulators, data converters, Gm-C filters, and many more uses. Optimization of analog integrated circuits especially OTAs is still the most exciting and laborious work in the area of circuit design. In [16], an ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing was designed in 0.35 µm CMOS technology. In [17], gm/ID methodology was presented for folded cascode OTA design in 0.35 µm CMOS technology. In [18], optimization of OTAs with power consumption minimization and noise optimization using ACO was presented. In this work, optimization of CMOS Miller OTA with rail to rail input/output swing using DE algorithm is presented. In section 2, DE algorithm

[1] *L. D. College of Engg., Gujarat Technological University-380005, India ORCID: 0000-0001-6731-4264*
[2] *VGEC, Chandkheda, Gujarat Technological University 380005, India ORCID: 0000-0003-2787-4608*
[3] *L. D. College of Engg., Gujarat Technological University 380005, India ORCID: 0000-0002-4683-1067*
** Corresponding Author: pp12479@yahoo.co.in*

is described. CMOS Miller OTA with rail to rail input/output swing is explained in section 3. Experimental setup for this work is presented in section 4. Simulation results found in this work are presented in section 5. Finally, in section 6, conclusions are discussed.

3. Differential Evolution Algorithm

Differential Evolution (DE) algorithm, proposed by Storn and Price [4], is a metaheuristic algorithm to solve the continuous parameter optimization problem. The DE algorithm uses the mutation, crossover, and selection strategies of GA. There are many mutation techniques for DE algorithm presented in the literature [4] [19]. The DE/rand/1/bin is the finest method to find the global optimal result [19]. It has been testified that DE gives better performance than PSO and GA for several numerical benchmark functions [20]. It has successfully been used in different areas of engineering and science, for example, machine intelligence, and signal processing, pattern recognition, power system optimization and many more others. In different literature, DE algorithm has also been presented to optimize CMOS based analog circuits design [8] [12]. DE algorithm uses N variables as the population of D dimensional parameter vectors for each generation [4]. The main steps of DE algorithm are given by flow chart in Fig. 1.

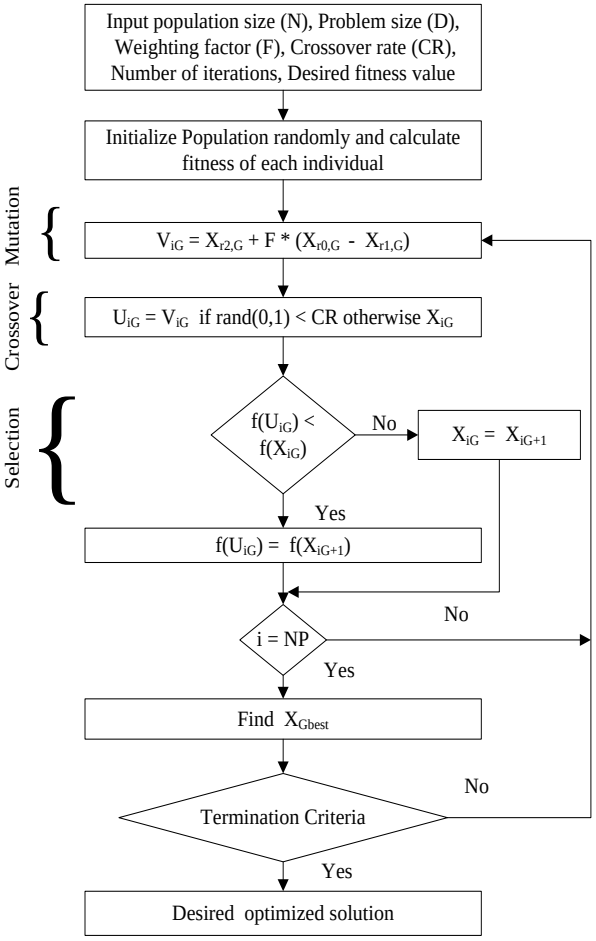

Fig. 1. Flowchart of the DE Algorithm.

In the above flowchart, input parameters such as population size (N), problem size (D), weighting factor (F), crossover rate (CR), number of iterations (G), and desired fitness value (F_{error}) are selected. If no constraints are set for the optimization problem, then the initial population is chosen at random. DE generates new design variables by adding up the weighted difference vector between two population members to a third population member. The process of DE algorithm is expressed mathematically by the following equation [4].

$$V_{iG} = X_{r2,G} + F * (X_{r0,G} - X_{r1,G}) \quad (1)$$

Here, X_{r0} and X_{r1} vectors are selected randomly, X_{r2} is another randomly chosen vector, subscript G is the iteration number, and F is a weighting factor. The weighting factor F is chosen in the optimal range of (0.5, 1) [19]. The main control parameters of the DE algorithm are F, N and crossover rate (CR) [19]. If the value of the randomly generated number between 0 and 1 within the CR limit, then crossover is carried out as shown in Fig 1. If the resultant vector yields a lower objective function value than previous population member, then the newly generated vector replaces the previous vector. The best parameter vector is calculated for every iteration in order to keep path of the progress made during the optimization process. This process is continue until termination criteria are fulfilled.

4. CMOS Miller OTA

An ideal operational transconductance amplifier (OTA) is a voltage-controlled current source with a constant transconductance and infinite input/output impedances. The main concerns of CMOS OTA are high linearity, high frequency, and low power. The OTA is used as main building block for different analog circuits and mixed-signal circuits. A variety of CMOS OTAs with different topologies have been reported for different applications [16], [17]. Here, optimization of a simple CMOS Miller OTA with rail to rail input out swing is presented using DE algorithm. The CMOS Miller OTA with rail to rail input/output swing is shown in Fig. 2, [13], [16]. It consists combining bulk-driven differential pair and dc level shifters. The main circuit design parameters of a CMOS based analog circuit are channel width (W) and channel length (L) of different NMOS and PMOS transistors, bias current, resistor value and capacitor value. This circuit has eleven design parameters namely W_1, W_2, W_3, W_4, W_5, W_6, W_7, W_8, R_c, C_c and bias current (I_{bias}) as observed in Fig. 2, so the dimension of the optimization problem (D) is 11. This circuit is claimed to have rail to rail input and output swing, for power supply as low as 600 mV, which is less than threshold voltages of transistors.

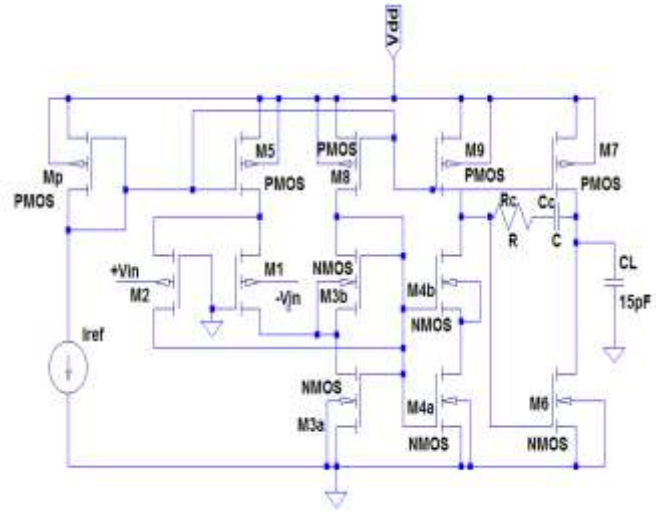

Fig. 2. CMOS Miller OTA [8]

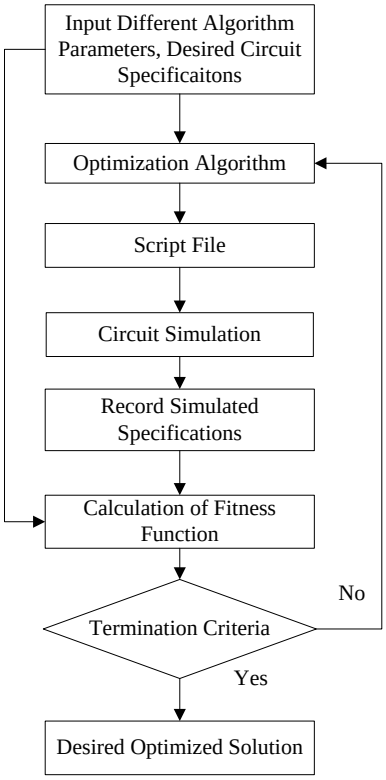

Fig. 3. Flow Diagram of Automatic Optimization Technique.

5. Experimental setup

The main steps of the automatic optimization technique are shown by the flow diagram in Fig. 3. This technique uses an optimization algorithm to generate circuit design parameters and a circuit simulator to produce simulation results for a specified CMOS based analog circuit. The error function is calculated based on simulation results produced by the circuit simulator. The error function (F_{error}) is defined by the following equation [11],

$$F_{error} = \sqrt{\sum_{j=1}^{M} \left(\frac{Spec_{Desired} - Spec_{Simulated}}{Spec_{Desired}}\right)_j^2} \quad (2)$$

Here, M is the number of specifications. The RMS error offers similar balancing to all the specifications. So, the optimizer tries to satisfy all the specifications similarly. If termination criteria are met, then the optimization procedure will stop. The termination criteria for this optimization procedure are the minimum value of the error function or a maximum number of iterations. For this work, the minimum value of F_{error} is considered as 1e-6. DE algorithm has been developed using C language and interfaced with ngspice circuit simulator tool. All experimentations have been performed on a core i5, 2.4 GHz processor, 4 GB RAM with Ubuntu operating system (OS). DE algorithm has generally three control variable settings of N, F, and CR. In this work, N = 10*D, F = 0.8 and CR = 0.5 are chosen [19].

6. Simulation Results and Discussion

In this work, automatic optimization of CMOS Miller OTA with rail to rail input/output swing is presented. This circuit has desired specifications as listed in Table 1.

Table 1. Desired Specifications of CMOS Miller OTA

Sr. No.	Desired Specifications
1	Open loo voltage gain (A_V) > 75 dB
2	Unit gain bandwidth (UGB) > 25 kHz
3	Phase margin (PM) > 45°
4	Power supply rejection ratio (PSSR) (+ve) > 60 dB
5	PSSR (- ve) > 60 dB
6	Rising slew rate (SR)> 10 V/ms
7	Falling SR > 10 V/ms
8	Common mode rejection ratio (CMRR) > 60 dB
9	DC power dissipation (P_{diss}) < 10 µW
10	Total MOS transistor area < 14500 µm^2

This circuit is simulated with 0.18 µm and 0.35 µm CMOS technology and biased with 0.6 supply voltage to operate in weak inversion region. Design parameters range and obtained parameters for this circuit using DE algorithm are listed in Table 2.

Table 2. Design parameters range and Obtained parameters using DE algorithm

Sr. No.	Design Parameters Rang	Obtained Parameters (0.35µm)	Obtained Parameters (0.180 µm)
1	W_1 = 1 to 200 µm	200/1 µm	120.19/1 µm
2	W_2 = 1 to 200 µm	70.72/1 µm	189.49/1 µm
3	W_3 = 1 to 200 µm	112.04/1 µm	199.30/1 µm
4	W_4 = 1 to 200 µm	142.55/9 µm	143.65/9 µm
5	W_5 = 1 to 200 µm	147.69/1 µm	32.68/1 µm
6	W_6 = 1 to 200 µm	200/9 µm	195.52/9 µm
7	W_7 = 1 to 200 µm	22.87/9 µm	19.68/9 µm
8	W_8 = 1 to 200 µm	84.28/9 µm	117.82/9 µm
9	R_c = 1 to 100 KΩ	100 KΩ	90.96 KΩ
10	C_c = 1 to 10 pF	1 pF	1 pF
11	I_{bias} = 1 to 10 µA	200 nA	190.76 nA

The simulation results of frequency response and CMRR with 0.18 µm CMOS technology are shown in Fig. 4 and Fig. 5. We can find an AV of 71.24 dB, UGB of 23.52 KHz and PM of 52.56° from Fig. 4. We can find a CMRR of 69.45 dB from Fig. 5.

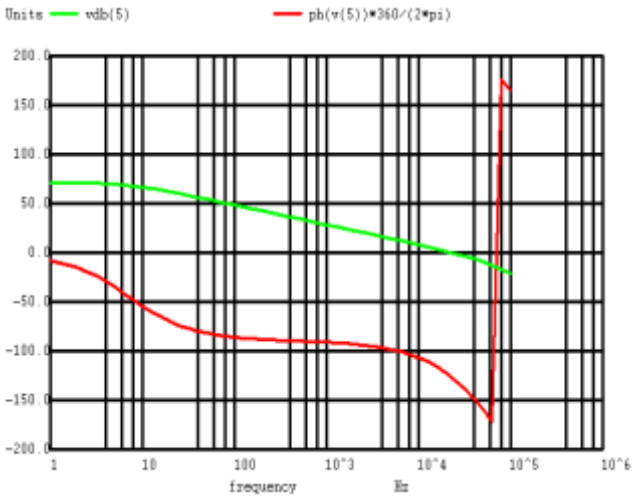

Fig. 4. Frequency Response of CMOS Miller OTA.

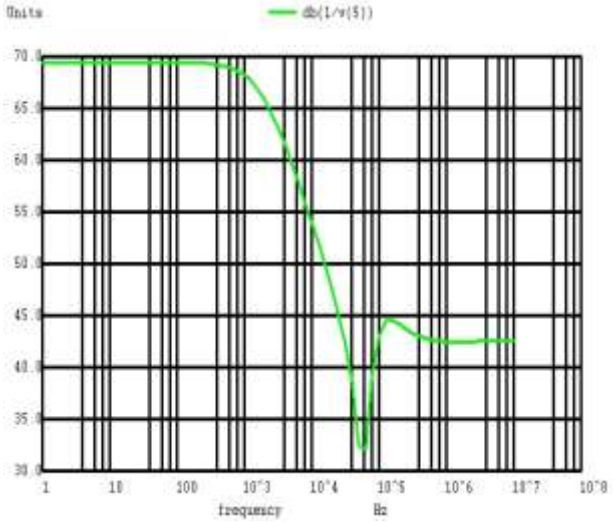

Fig. 5. CMRR of CMOS Miller OTA

The simulation results of PSSR (+ve) and PSSR (-ve) with 0.18 µm CMOS technology are shown in Fig. 6 and Fig. 7. In Fig. 6, PSSR (+ve) is 111.12 dB and in Fig. 7, PSSR (-ve) is 89.07 dB.

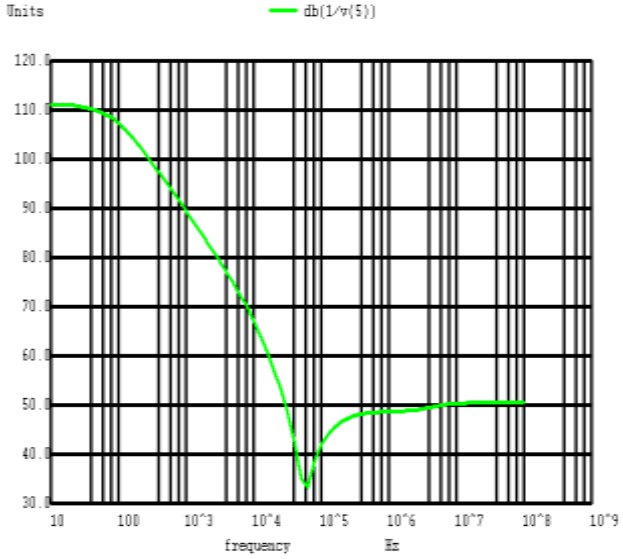

Fig. 6. PSSR (+ve) of CMOS Miller OTA.

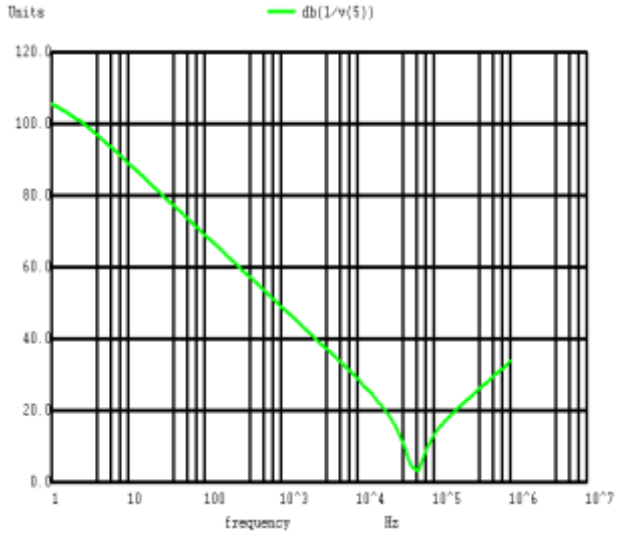

Fig. 7. PSSR (-ve) of CMOS Miller OTA.

The simulation result of the output waveform with 0.18 µm CMOS technology is shown in Fig. 8. This waveform is used to measure rising slew rate and falling slew rate. In Fig. 8, rising slew rate is 13.16 V/ms and falling slew rate is 30.84 V/ms.

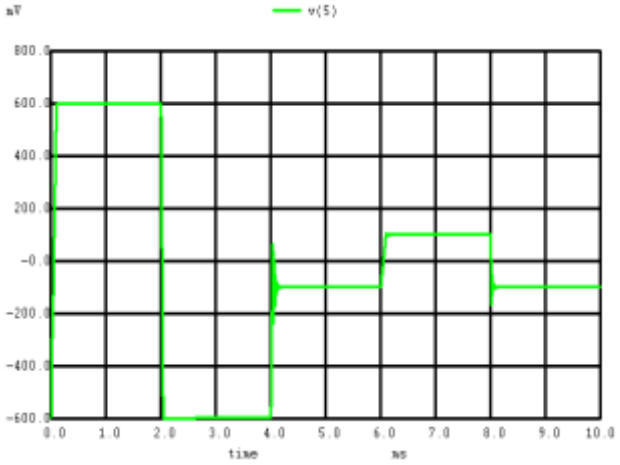

Fig 8. Output waveform of CMOS Miller OTA

The obtained simulation results with 0.18 µm CMOS technology in comparison with previously reported works are summarized in Table 3. From Table 3, we can observed that this circuit design using DE algorithm with 0.18 µm CMOS technology is satisfied all desired specifications with only 294 nW power consumption. The obtained simulation results with 0.35 µm CMOS technology in comparison with previously reported works are summarized in Table 4. From Table 4, we can observe that this circuit design using DE algorithm with 0.35 µm CMOS technology is satisfied all desired specifications with only 379 nW power consumption and 4577 µm2 total transistor area.

Table 3. Obtained simulation results in comparison with previously reported works for 0.18 µm CMOS technology

Sr. No.	Desired Specifications	Obtained Specifications (This work)	[13]	[11]
1	A_V > 75 dB	71.24 dB	91.39 dB	75 dB
2	UGB > 25 kHz	23.52 kHz	145.549 kHz	58 kHz
3	PM > 45°	52.56°	68.87°	59.7°
4	PSSR (+ve) > 60 dB	111.12 dB	124.48 dB	--
5	PSSR (- ve) > 60 dB	89.07 dB	104.81 dB	-
6	Rising SR > 10 V/ms	13.16 V/ms	11.9 V/ms	30.87 V/ms
7	Falling SR > 10 V/ms	30.84 V/ms	17.61 V/ms	16.4 V/ms
8	CMRR > 60 dB	69.45 dB	124.38 dB	--
9	P_{diss} < 10 µW	294 nW	14.92 µW	571 nW
10	Total MOS transistor area < 14500 µm^2	4831 µm^2	4839.8 µm^2	4598 µm^2

Table 4. Obtained simulation results in comparison with previously reported works for 0.35 µm CMOS technology

Sr. No.	Desired Specifications	Obtained Specification (This work)	[11]	[13]	[16]
1	A_V > 75 dB	76.52 dB	82.67 dB	77.71 dB	73.5 dB
2	UGB > 25 kHz	23.37 kHz	48.61 kHz	34.44 kHz	42.27 kHz
3	PM > 45°	70.24°	58.01°	89.24°	54.1°
4	PSSR (+ve) > 60 dB	112.77 dB	--	71.11 dB	--
5	PSSR (- ve) > 60 dB	88.27 dB	-	90.70 dB	-
6	Rising SR > 10 V/ms	13.13 V/ms	21.77 V/ms	12.58 V/ms	14.7 V/ms
7	Falling SR > 10 V/ms	39.34 V/ms	23.11 V/ms	72.73 V/ms	14.7 V/ms
8	CMRR > 60 dB	104.00 dB	--	85.27 dB	--
9	P_{diss} < 10 µW	379 nW	545.49 nW	9 µW	550 nW
10	Total MOS transistor area < 14500 μm^2	4577 μm^2	5586 μm^2	5033 μm^2	14500 μm^2

7. Conclusion

In this paper, DE algorithm is used to optimize CMOS Miller OTA with rail to rail input/output swing with 0.18 µm and 0.35 µm CMOS technology. This circuit is biased with 0.6 supply voltage to operate in weak inversion region. Compared to the previous works reported, DE algorithm optimized this circuit with 0.18 µm CMOS technology with less power consumption. We have also obtained less power consumption and less total transistor area in comparison to previous works reported in the literature for 0.35 µm CMOS technology. This circuit is suitable in ultra-low-power applications.

As a future work other recently developed nature-inspired algorithms can be tested to optimize the CMOS miller OTA and compared their performance with DE algorithm. The performance of an analog circuit is altered with Process (P), Voltage (V), and Temperature (T). PVT variations can be considered during optimization process of an analog circuit to develop a robust optimizer.

References

[1] A. C. Kammara, L. Palanichamy, and A. König, "Multi-objective optimization and visualization for analog design automation," *A. Complex Intell. Syst*., vol. 2, no. 4, pp. 251-267, Dec. 2016, https://doi.org/10.1007/s40747-016-0027-3.

[2] J. Kennedy and R. C. Eberhart, "Particle swarm optimization," at *Proceedings IEEE international conference on neural networks*, Perth, Australia, pp. 1942-1948, vol.4, 1995. doi: 10.1109/ ICNN.1995.488968.

[3] Darwin, Wim Kruiskamp DL, "CMOS OPAMP synthesis by means of a genetic algorithm," at *32nd conference on design automation, DAC '95,* San Francisco, CA, 1995, doi: 10.1145/217474.217566.

[4] R. Stron and K. Price, "Differential evolution- a simple and efficient heuristic for global optimization over continuous spaces," *Journal of Global Optimization*, vol. 11, no. 4, pp. 341-359, Dec. 1997, https://doi.org/10.1023/A:1008202821328.

[5] Z. W. Geem, J. H. Kim and G. Loganathan, "A new heuristic optimization algorithm: harmony search," *Simulation*, vol. 76, no. 2, pp. 60-68, Feb. 2001, https://doi.org/10.1177/0037549701076 00201.

[6] M. Dorigo, V. Maniezzo and A. Golomi, "Ant system: optimization by a colony of cooperating agent," *IEEE Trans. System, Man, and Cybernetics*, vol. 26, no. 1, pp. 29-41, Feb. 1996, DOI:10.1109/3477.484436.

[7] D. Karaboga, "An idea based on honey bee swarm for numerical optimization," Erciycs University, Engineering Faculty, Computer Engineering Dept., Technical Report-TR-06, Oct. 2005. Available: http://www.dmi.unict.it/mpavone/nc-cs/materiale/tr06_2005.pdf

[8] S. Sabat, K. Kumar, and S. Udgata, "Differential evolution and swarm intelligence techniques for analog circuit synthesis 2009," at *World congress on nature biologically inspired computing, NaBIC*, Coimbatore, India, pp. 469-475, Dec.2009, doi: 10.1109/NABIC. 2009.5393356

[9] R. Vural and U. Ayten, "Optimized analog filter approximation via evolutionary algorithms," at *12th international conference on intelligent systems design and applications (ISDA)*, Kochi, India, pp. 485-490, Nov. 2012, doi: 10.1109/ISDA.2012.6416586.

[10] S. Kudikala, S. L. Sabat and S. K. Udgata, "Performance study of harmony search algorithm for analog circuit sizing," at *International symposium on electronic system design (ISED)*, Kerala, India, pp. 12-17, Dec. 2011, doi: 10.1109/ISED.2011.42.

[11] R. A. Thakker, M. Baghini, and M.Patil "Low-power low-voltage analog circuit design using hierarchical particle swarm optimization," at *22nd international conference on VLSI design*, pp. 427-432, Jan. 2009, doi:10.1109/VLSI.Design.2009.14.

[12] S. Sharma, and P. P. Prajapati, , "Design of Various Analog Circuits using Differential Evolutionary Algorithm," *International Journal of Scientific Progress and Research,* vol. 23, no. 3, pp. 159-165, May 2016.

[13] P. P. Prajapati and M. V. Shah, "Automated Sizing Methodology for CMOS Miller Operational Transconductance Amplifier," *Soft Computing: theories and applications, Advances in Intelligent Systems and Computing*, vol. 584, pp 301-308, Springer, Singapore, Nov. 2017, DOI.org/10.1007/978-981-10-5699-4_29

[14] S. Patel, and R. A. Thakkar, "Automatic Circuit Design and Optimization using Modified PSO Algorithm," *Journal of Engineering Science and Technology Review*, vol. 9, no. 4, pp. 192-197, Sep. 2016.

[15] P. P. Prajapati, and M. V. Shah, "Two Stage CMOS Operational Amplifier Design Using Particle Swarm Optimization Algorithm," at *IEEE UP Section Conference on Electrical Computer and Electronics*, 2015.

[16] L. Ferreira, C. P. Tales, and L. M. Robson, "An ultra-low-voltage ultra-low-power CMOS Miller OTA with rail-to-rail input/output swing," *IEEE Transctions on Circuits and Systems.-II: Exp. Briefs*, vol. 54, no. 10,Oct. 2007, DOI :10.1109/TCSII.2007.902216.

[17] H. D. Dammak, S. Bensalem, S. Zouari, and M. Loulo, "Design of Folded Cascode OTA in Different Regions of Operation through gm/ID Methodology," *World Academy of Science,Engineering and Technology, International Journal of Electrical, Computer, Energetic, Electronic and Communication Engineering*, vol. 2, no. 9, pp. 174-176, 2008.

[18] M. Akbari, M. Shokouhifar, O. Hashemipour, et al., "Systematic design of analog integrated circuits using ant colony algorithm based on noise optimization," *Analog Integr. Circ. Sig. Process.*, vol. 86, no. 2, pp. 327-339, Feb. 2016, https://doi.org/10.1007 /s10470-015-0682-0.

[19] V. Arunachalam, "Optimization using Differential Evolution," Facility for Intelligent Decision Support, Department of Civil and Environmental Engineering, London, Ontario, Canada., Water Resources Research Report no. 60, July 2008, Available: https://ir.lib.uwo.ca/cgi/viewcontent.cgi?article=1022&context= wrrr.

[20] S. Dasgupta, S. Das, A. Biswas, and A. Abraham, "On Stability and Convergence of the Population-Dynamics in Differential Evolution," *The European Journal on Artificial Intelligence,* vol. 22, no.1, pp. 1-20, Jan. 2009.

[21] H. Gupta and B.Ghosh, "Analog Circuits Design using Ant Colony Optimization," *International Journal of Electronics, Computer & Communications Technologies*, vol. 2, no.3, pp. 9-21, April. 2012.